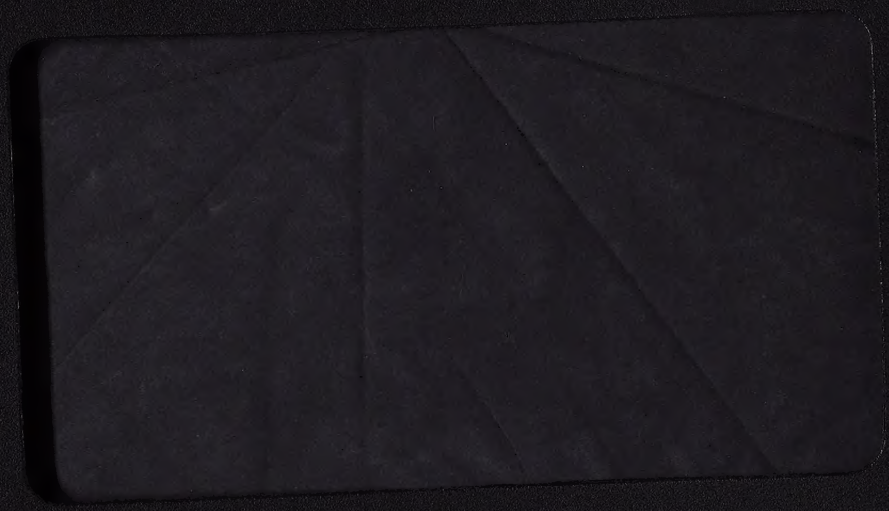
INSTRUCTION MANUAL
SD112-H

VOLTMETER/LOG CONVERTER

(MODIFIED TO MODEL SD112-1-H-3)

Spectral Dynamics

Scientific-Atlanta



SERIAL 421

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Spectral Dynamics

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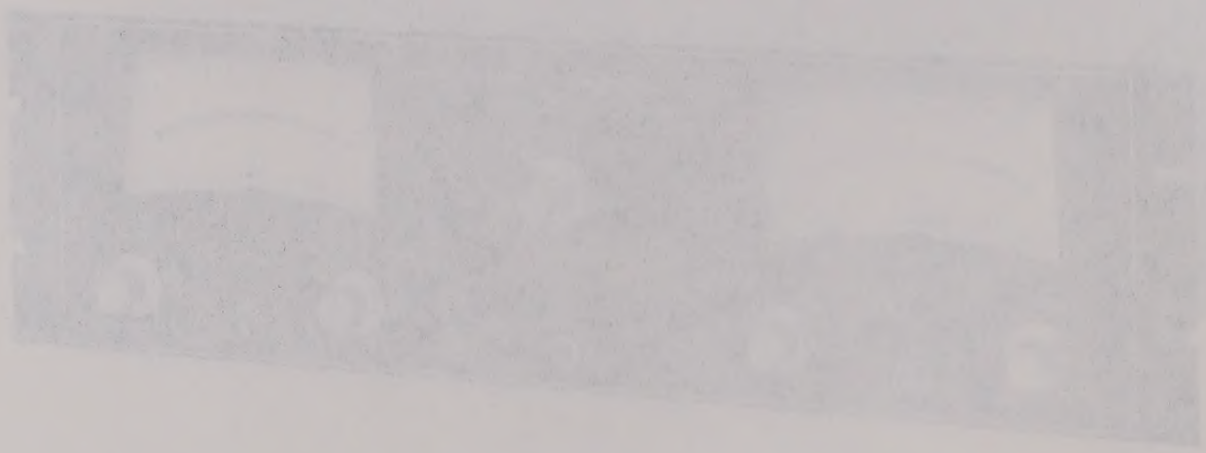
December 1977

MODEL SD112-H VOLTMETER/LOG CONVERTER



ADDENDUM

Model SD112-1-H-3 Voltmeter/Frequency Log Converter

The Model SD112-1-H-3 is basically a standard SDC Model SD112-1-H Voltmeter/Frequency Log Converter. The "-3" added to the basic model number denotes a modification designed to provide a frequency response rolloff of 1 dB at 5 Hz and 0.5 dB at 6 Hz.

Internal changes resulting from this modification involved the following components as indicated:

Component	From	To
C3 & C4	2 μF	20 μF
C7 & C8	10 μF	20 μF
A1C33 & A9C33	2 μF	4 μF
A1C34 & A9C34	0.47 μF	1 μF

HARDWARE
WARRANTY POLICY

All products manufactured by Spectral Dynamics are warranted against defects in materials and workmanship for one year from the date of delivery or, in the case of certain components listed in some of the operating manuals, for the specified period. We will repair or replace products which prove defective during the warranty period, providing the failure or damage has not been caused by misuse or abnormal operating conditions.

If the malfunction or a portion thereof is determined by Spectral Dynamics Corporation to have been caused by misuse or abnormal conditions of operation, an estimate of cost to repair will be submitted to the purchaser for approval before beginning any repair work.

Computers, computer accessories and other equipment made by other manufacturers and sold by Spectral Dynamics for use with its instruments are specifically excluded from this warranty. Spectral Dynamics encourages buyers of systems which include computer equipment to obtain Service Agreements with the computer manufacturer. We are happy to assist in this regard.

Liability under this warranty is limited to servicing and adjusting the instrument returned to the Spectral Dynamics Corporation factory, with transportation charges prepaid by the purchaser. NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. WE ARE NOT LIABLE FOR CONSEQUENTIAL DAMAGES.

If a malfunction develops, notify the Customer Service Department of Spectral Dynamics Corporation or its representative in your area, giving details of the problem and the name, model and serial number of the equipment. Upon receipt of this information, service data or shipping instructions will be provided.

Spectral Dynamics Corporation
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S-072
August 1977

PREFACE

RECEIVING INSPECTION PROCEDURE

The Model SD112-H Voltmeter/Log Converter is shipped in a manner designed to protect it against normal shipping hazards. Immediately upon receipt, inspect and note any apparent visible damage. Keep all forms and invoices. Test its operation and if shipping damage is apparent, file a claim with the carrier's claims agent and send a copy to Spectral Dynamics Corporation. Be sure to include the system name, model number, and serial number on all correspondence. Spectral Dynamics Corporation will advise the buyer what should be done; arrangements for repair or replacement will be made as applicable.

RETURN SHIPMENT PROCEDURE

On receipt of shipping instructions, forward the instrument prepaid via air freight to the factory or authorized repair station indicated on the instructions. Replace the instrument in its original shipping case or equivalent container.

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SECTION I

GENERAL INFORMATION

1.1 INTRODUCTION

The Model SD112-H Voltmeter/Log Converter is an all solid-state, electronic, two-channel, a-c (rms), d-c voltmeter and log converter. Each channel measures up to 100 Vrms ac or dc, displays it in both rms volts and relative dB level on a front panel meter, and provides a d-c output (10 mV/dB) proportional to the log of the rms input.

Typical applications for the SD112-H Voltmeter/Log Converter are as follows:

a. Transfer Function Analysis, Magnitude and Phase

b. Mechanical Impedance Studies

c. Transmissibility and System Response Analysis

d. Random Signal Analysis

Detailed information for the use of the SD112-H in various applications is given in Section II of this manual.

The additional function of log frequency conversion is available in the Model SD112-1-H Voltmeter/ Frequency Log Converter. In addition to the voltmeter and log conversion functions of the Model SD112-H, the Model SD112-1-H will accept any shape periodic waveform, sine wave to pulse, over the frequency range of 5 Hz to 20 kHz (in three decade intervals) and provide two d-c outputs (0 to 1V, and 0 to 0.1V), each proportional to the log of the input frequency over the selected range.

The Model SD112-H can be modified to include the log frequency converter circuit. However, this is a factory-type modification that requires the installation of a new front panel, the log frequency converter circuit card, additional rear panel connectors, and considerable internal wiring and cabling. For further details, contact an SDC factory representative.

1.2 BASIC OPERATION

Both channels operate the same; therefore, only one is described and shown in Figure 1-1.

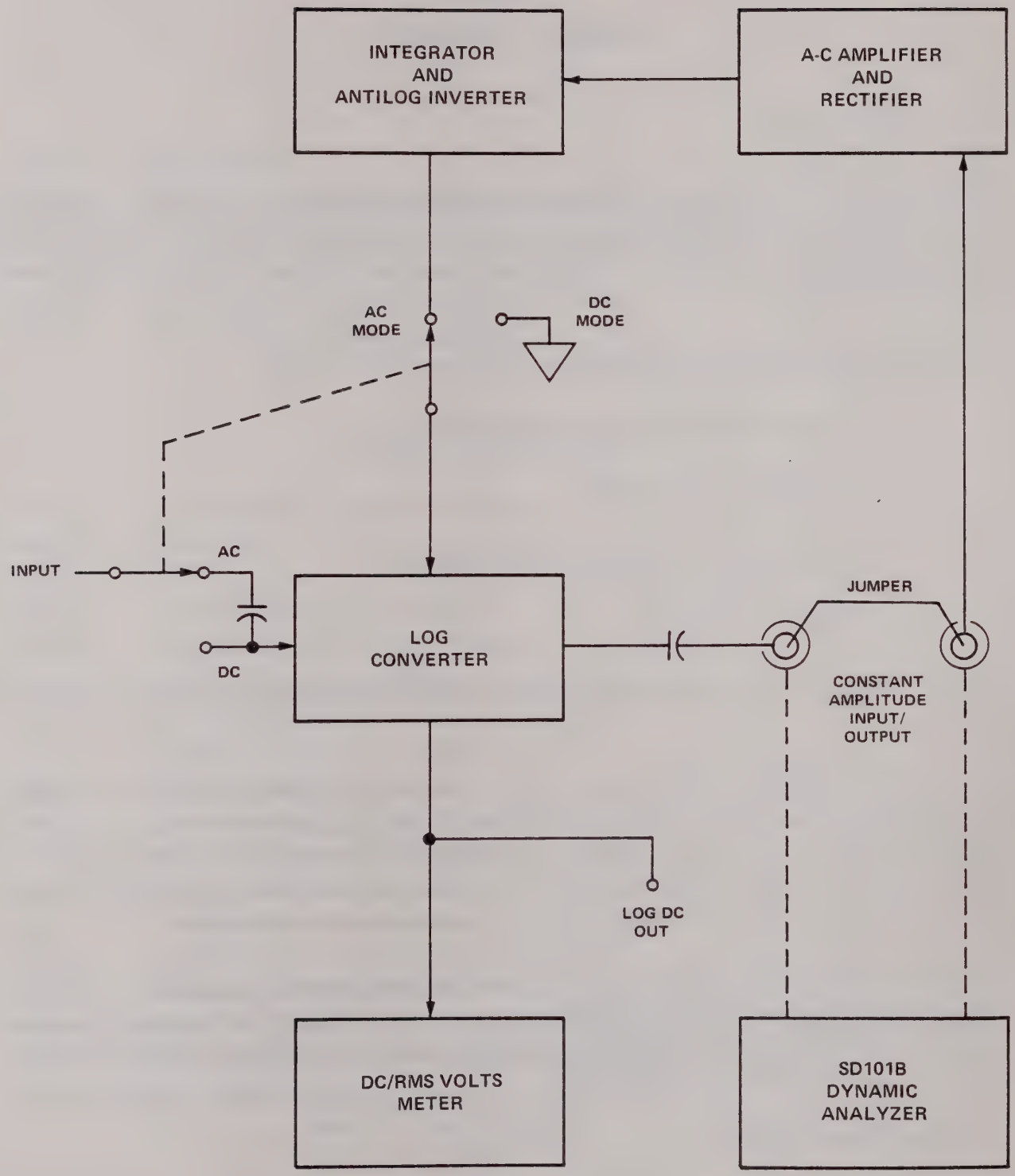


Figure 1-1. Simplified Block Diagram (One Channel)

In the d-c mode of operation, a d-c input is converted to a voltage proportional to its logarithm, which is applied to the front panel meter and LOG DC OUT connector.

In the a-c mode of operation, an a-c input passes through the log converter, into an electronic servo loop. Here it is amplified and then rectified. The d-c voltage produced is amplified, integrated and inverted, and then applied to the log converter. The d-c output of the log converter is equal to the log of the rms value of the a-c input. This voltage is applied to the front panel meter and LOG DC OUT connector.

A narrowband or single frequency of a wide spectrum (10 Hz to 20 kHz) can be selected and accurately measured by interconnecting an SD101B Dynamic Analyzer (tracking filter) to the CONSTANT AMPLITUDE OUTPUT/INPUT connectors.

1.3 FRONT PANEL FUNCTIONAL DESCRIPTION

Figure 1-2 shows the instrument front panel followed by keyed brief descriptions of each of the front panel functions.

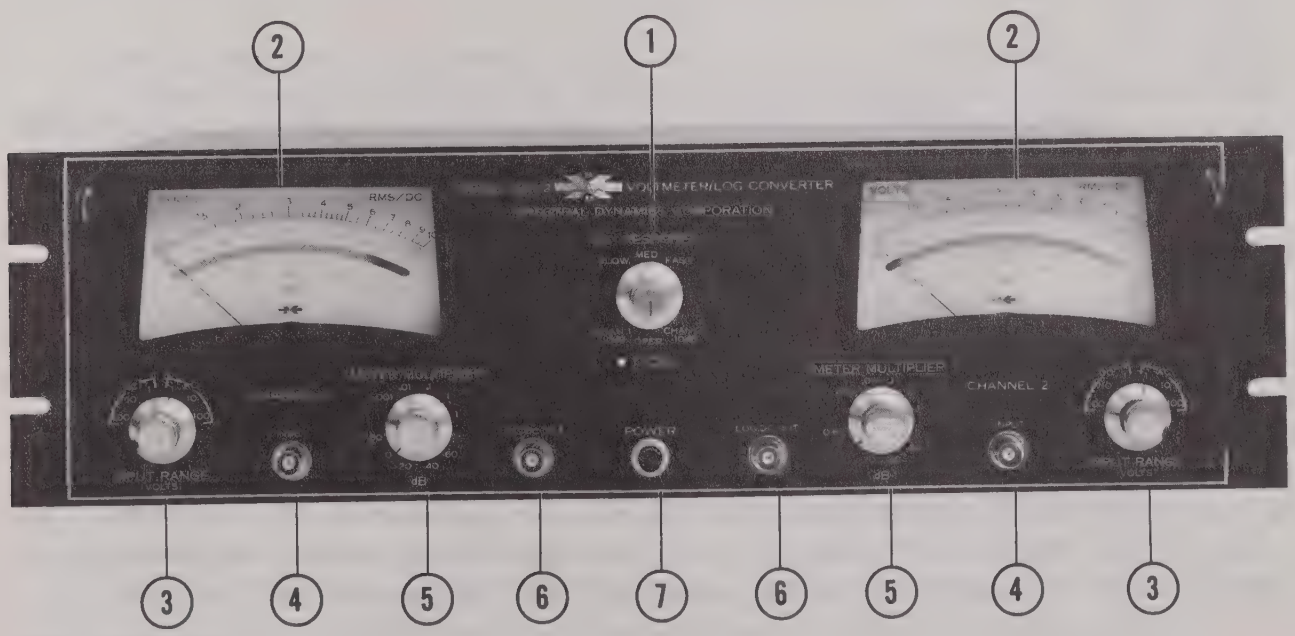


Figure 1-2. Front Panel

(1) RESPONSE/Y-CAL

This dual control switch performs the following two functions:

RESPONSE

Outside (larger) knob of this switch selects slow, medium, or fast response time of the instrument as dictated by the input-signal excursion time. For stability, the instrument should be the slowest integral part of a system. For example, in an impedance measuring system using an SD101B Dynamic Analyzer, the associated tracking-filter-bandwidth governs this switch setting. For a filter bandwidth between 2 to 10 Hz, 10 to 20 Hz, or 20 to 200 Hz, set this switch to SLOW, MED, or FAST respectively.

Y-CAL

Inside (smaller) knob of this switch provides for insertion of a precision 10 dB attenuator into the circuitry of either Channel 1 or 2. The resultant –100 mVdc change in the instrument output level may be used to calibrate peripheral equipment, particularly X-Y recorders. When not calibrating, set Y-CAL switch to OPER.

(2) VOLTS RMS/DC METER

Indicates the RMS voltage amplitude and dB level of the input signal in ranges determined by the INPUT RANGE and METER MULTIPLIER switch settings. The bottom 0—80 dB scale allows monitoring signals varying over a wide dynamic range. The center 20 dB scale in conjunction with the METER MULTIPLIER switch provides four expanded 20 dB ranges incremented over the full 80 dB range. In each expanded range, the dB level of the measured voltage is referenced to full scale as determined by the INPUT RANGE and METER MULTIPLIER switch settings. In like manner, the top scale simultaneously indicates the rms voltage level.

(3) INPUT RANGE (VOLTS)

Setting determines the a-c or d-c input voltage range of the instrument. The three AC ranges (1, 10 and 100V) are used when measuring the rms value of a-c input signal voltages having sinusoidal or complex waveforms. The three DC ranges (1, 10 and 100V) are used when measuring d-c input voltages (positive polarity), either steady state or dc with an a-c component. Automatic overload protection is provided on all input ranges.

(4) INPUT

Used to apply a-c or d-c (negative ground) inputs to the instrument. When the instrument is used in a system, inputs are normally applied through the AUX FUNCTIONS connector on the rear chassis panel (see Figure 1-3), and this INPUT can be used for monitoring the input signal.

(5) METER MULTIPLIER

Setting determines the computing factor to be used with the METER reading to obtain actual voltage magnitude or dB level of the input signal voltage. Except for the 0—80 dB setting which provides full 80 dB dynamic range of the instrument as read on the bottom METER scale, the double-lined knob indicates both the voltage-scale multiplier factor (top markings) to be used with the top METER scale, and the dB level (bottom markings) to be algebraically added to the reading of the center 20 dB METER scale. (Refer to paragraph 2.4.)

(6) LOG DC OUT

Used for connecting the output (a d-c voltage proportional to the logarithm of the input signal) of the SD112-H to recording or other peripheral test equipment. When the SD112-H is used in a system, the output is normally taken from the AUX FUNCTIONS connector on the rear chassis panel (see Figure 1-3), and this connector can be used for monitoring the log d-c output voltage.

(7) POWER

Push button type switch/indicator used to turn instrument on and off. Push button glows red when power is on.

1.4 REAR OF CHASSIS FUNCTIONAL DESCRIPTION

Figure 1-3 shows the rear of the chassis followed by keyed brief descriptions of each of the inputs and outputs.

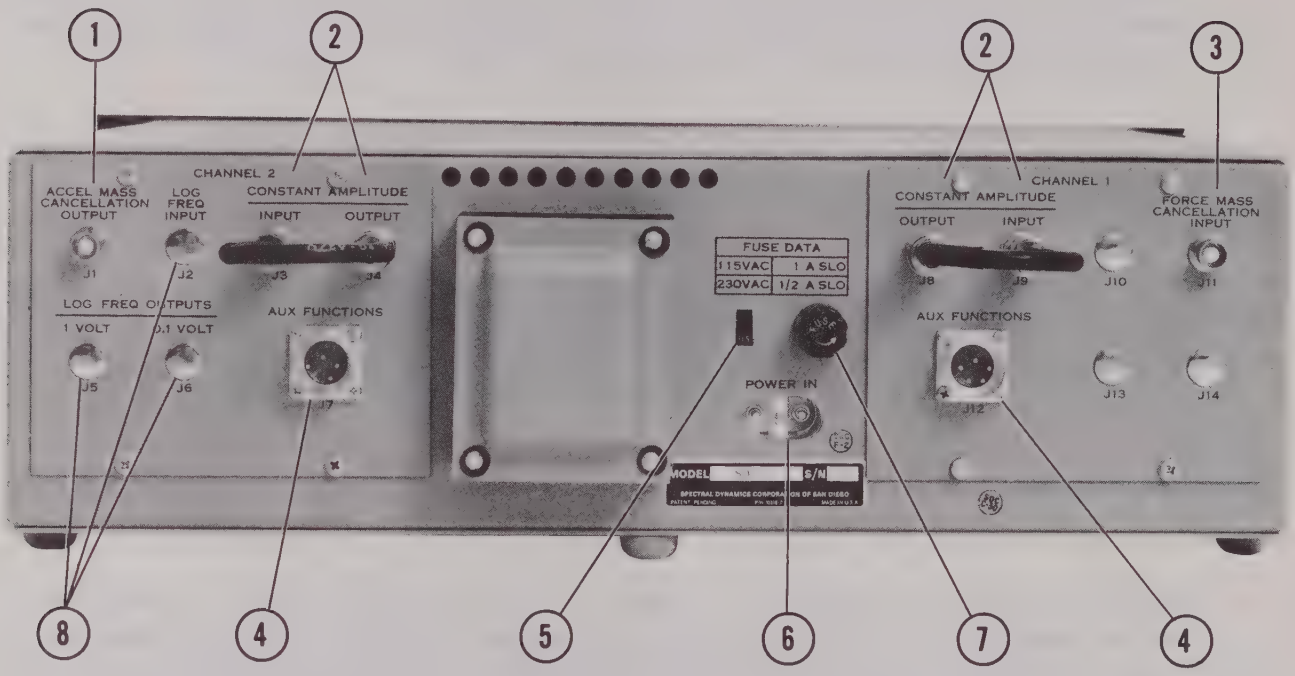


Figure 1-3. Rear of Chassis

(1) ACCEL MASS CANCELLATION OUTPUT

This output is used only when the SD112-H is part of an Automatic Mechanical Impedance Measuring System such as the SD1002 System produced by SDC. Use of this output is covered in the system manual and in Paragraph 3.4.2.1 of this manual.

(2) CONSTANT AMPLITUDE INPUT/OUTPUT

Jumpered by short coaxial cable when the instrument is used as a broadband voltmeter/log converter. Allows insertion of a filter when measuring noisy a-c signals. In system use, an SD101B Dynamic Analyzer can be inserted here to track a swept-frequency a-c input signal at a controlled bandwidth thus allowing the measurement and log conversion of fundamental or narrow bandwidth signals.

(3) FORCE MASS CANCELLATION INPUT

This input is used in conjunction with No. 1 above. Refer also to paragraph 3.4.2.1 of this manual.

(4) AUX FUNCTIONS

Provides input and output connections at rear of instrument when used in a system (rack-mounted in cabinet). Terminal 1 is signal input; 2 is circuit ground; and 3 is log d-c output.

(5) 115/230 Switch

Facilitates changeover of primary power input circuit for either 115V or 230V operation. Proper input power to be applied shows in window; screwdriver blade slot is up for 115V operation and down for 230V operation.

(6) POWER IN

Accepts 3-wire plug and cable (supplied) for applying 115/230V a-c 50—60 Hz primary input power. Center terminal is chassis ground. Uses Belden No. 17258-S cable (as used on most Hewlett-Packard instruments, and obtainable from normal sources of HP parts).

(7) FUSE

Contains 3AG type, SLO-BLO fuse; 1A for 115V operation or 1/2-A for 230V operation.

(8) Not used. Reserved for Model SD112-1 Voltmeter/Frequency Log Converter.

1.5 SPECIFICATIONS

The Model SD112-H Voltmeter/Log Converter has been calibrated for conformance to the following specifications:

Input

Mode	ac or dc
Frequency	10 Hz to 10 kHz; down approximately 0.5 dB from full scale at 20 kHz

Ranges	1, 10 and 100 Vrms or dc, full scale
Impedance	100kΩ
Crest Factor	4:1 at full scale, 5:1 at 4/5 full scale and below
Output	Nominally 10 mV/dB; +400 mV ≅ 0 dB, 0 mV ≅−40 dB, −400 mV ≅−80 dB
Accuracy	±0.5 dB over 80 dB range, from 10 Hz to 10 kHz with SDC Tracking Filter
	±0.5 dB over 60 dB range, from 10 Hz to 10 kHz without SDC Tracking Filter
Impedance	1kΩ nominal
A-C Response	Nominally 8 dB/s; 40 dB/s and 80 dB/s switch selectable
Meter Accuracy	±2 dB, 0–80 dB scale, 10 Hz to 10 kHz with SDC Tracking Filter
	±2 dB, 0 to 60 dB on 0–80 dB scale, 10 Hz to 10 kHz without SDC Tracking Filter
Expanded Meter Scales	AC Mode:
	±0.5 dB over 70 dB range, from 10 Hz to 10 kHz with SDC Tracking Filter; useful to 80 dB
	±0.5 dB over a 0 to 60 dB dynamic range, from 10 Hz to 10 kHz without SDC Tracking Filter
	DC Mode:
	±0.5 dB over a 0 to 50 dB dynamic range; useful to 60 dB
Phase Coherency	Channels phase-matched to within ±2 degrees over 10 Hz to 10 kHz frequency range

Calibration	Scales calibrated in Vrms and dc, and in dB with reference to full scale for sine waves; rms detector provides less than 4% additional error for periodic waveform with duty cycle greater than 0.3 or stationary random waveforms with crest factors not greater than 3.5 to 1 at full scale.
Power	115/230V a-c, 50/60 Hz, at approximately 25W
Inputs/Outputs	INPUT and LOG DC OUT connectors on front panel are in parallel with AUX FUNCTIONS connector on rear panel
Dimensions	Height . . . . . .(13,3 cm) 5-1/4"
	Width (std. panel) . . . . . (48,3 cm) 19"
	Depth (w/o connectors) . . . . . (35,6 cm) 14"
	Weight . . . . . .(9,06 kg) ≈20 lb

1.6 PRINTED CIRCUIT CARDS

Except for the circuit card extender board, each printed circuit card is individually keyed to its receptacle. The circuit cards alphanumerical reference designations match the receptacle designations; i.e., board A1 plugs into J1, board A2 plugs into J2, etc.

1.7 EXTENDER BOARD

The 22-pin circuit card extender board, when not in use, plugs into a spare receptacle on top of the chassis. For troubleshooting and calibration purposes, the extender board may be plugged into a selected receptacle, with the regular printed circuit card assembly mounted on top, thus making the various test points easily accessible. Before inserting the extender board in a receptacle, remove the nylon key insert from the receptacle with a long-nose pliers. When tests are completed and the extender board has been removed, replace the key insert in its proper place adjacent to the black dot on the circuit plate.

SECTION II

OPERATION

2.1 INTRODUCTION

This section provides instructions for operating the SD112-H Voltmeter/Log Converter. Either or both channels of the instrument can be used as separate instruments or in a system to measure d-c or a-c rms voltages. Each channel also provides a d-c output that is proportional to the log of the rms value of the input signal.

2.2 CONTROLS, INDICATORS AND CONNECTORS

All controls, indicators and connectors are identified and their operations are described on Figures 1-2 and 1-3 in Section I of this manual.

2.3 TURN-ON PROCEDURE

a. Check that 115/230 switch on instrument rear panel is set to proper input line voltage.

b. Plug power cord (Belden No. 17258-S supplied) into POWER IN receptacle on instrument rear panel and connect to primary power receptacle.

c. Press POWER switch/indicator on front panel; it should glow red indicating power is on.

NOTE

Allow at least 30 minutes for the instrument to warm up and stabilize.

2.4 OPERATING INSTRUCTIONS

NOTE

If it is desired to operate the instrument with the signal input circuit ground isolated from the instrument chassis ground, remove the jumper between CIRCUIT GND and CHASSIS GND terminals on rear panel. (See Figure 1-3.)

2.4.1 Use as a DC or RMS Voltmeter

To operate either or both channels of the SD112-H as a d-c or rms voltmeter, proceed as follows:

a. Ensure that jumpers are connected from INPUT to OUTPUT of CONSTANT AMPLITUDE connectors on rear panel.

b. Set RESPONSE switch to MED, and Y-CAL switch to OPER.

c. Set INPUT RANGE (VOLTS) switch to 100 (a-c or d-c mode depending on expected signal).

NOTE

If it is desirable to read the a-c component of a d-c signal, operate instrument in a-c mode.

d. Set METER MULTIPLIER switch to 1. With INPUT RANGE set to 100, full scale meter reading is 100 Vdc or Vrms.

e. If indication is not convenient to read (needle at extreme left end of scale), change setting of METER MULTIPLIER and INPUT RANGE switch to provide progressively lower meter scaling. Table 2-1 gives the INPUT RANGE and METER MULTIPLIER switch settings versus full-scale meter readings.

Table 2-1. Meter Scaling

INPUT RANGE (VOLTS) AC or DC	METER MULTIPLIER	FULL-SCALE READING
100	1	100
	.1	10
	.01	1
	.001	.1
10	1	10
	.1	1
	.01	.1
	.001	.01
1	1	1
	.1	.1
	.01	.01
	.001	.001

2.4.2 Use as a dB Meter

The meter provides continuous voltage level readings in dB as well as rms volts on all ranges. (See Figure 1-2.)

With the METER MULTIPLIER switch set to 0—80/1 (bottom/upper markings), the meter provides full dynamic range of 80 dB for any setting of the INPUT RANGE switch; that is, full scale is always 0 dB as referenced to the particular full-scale input.

Changing the setting of the METER MULTIPLIER switch to any of the other four settings provides an expanded 20 dB segment of the overall range. For the dB level relative to the INPUT RANGE setting, read the center 20 dB meter scale as a negative value and algebraically add the value (0, -20, -40, or -60) indicated by the METER MULTIPLIER switch (lower markings). Now the meter reads the input voltage level in -dB relative to the full-scale meter voltage; full-scale meter voltage (see Table 2-1) equals the INPUT RANGE times the METER MULTIPLIER (top markings). For example:

INPUT RANGE:	10 DC
METER MULTIPLIER:	.1 (top marking)/-20 dB (bottom marking)
Meter Reading:	(-) 8 dB (center scale)

For this example, the voltage level in dB is -28 dB [(-)8 + (-20)] referenced to 10V (INPUT RANGE setting), or -8 dB [(-) meter] reading referenced to 1V (INPUT RANGE x METER MULTIPLIER).

A second example follows:

INPUT RANGE:	1 AC
METER MULTIPLIER:	.01/-40 dB
Meter Reading:	(-) 12

For this example, the voltage level in dB is -52 dB referenced to 1V, or -12 dB referenced to 0.01V.

2.4.3 Use as a Log Converter

The instrument continuously provides a d-c output (10 mV/dB) at the LOG DC OUT connector, that is proportional to the log of the rms value of the input signal. This output can be used to drive an X-Y recorder, digital voltmeter, or other recording device.

The LOG DC OUT voltage (nominal) for full-scale meter reading on any range (1, 10 or 100) is +400 mV; for full scale -40 dB, it is 0V; and for full scale -80 dB, it is -400 mV. Consult the instruction manual for the recording device to be used and determine its applicable input voltage levels.

2.4.4 Recorder Y-Axis Calibration

The Y-CAL switch provides a calibrated -10 dB level; that is, changes the LOG DC OUT voltage level by -10 dB as referenced to the INPUT signal. To calibrate an external recording device, proceed as follows:

a. Interconnect the instrument LOG DC OUT to the input of the recording device. (Refer to instruction manual for particular recorder being used.)

b. Apply a fixed INPUT signal level to the SD112-H. Note the output level indicated by the recorder.

c. Set the Y-CAL switch to CHAN 1 -10 dB or CHAN 2 -10 dB, as applicable for channel being used.

d. Note new output level indicated by recorder, and adjust recorder controls as necessary for a -10 dB level change from that noted in step b.

e. Both channels are calibrated in the same manner as outlined in steps a. through d. above. After calibration is complete, return the Y-CAL switch to OPER.

2.5 SYSTEM OPERATING INSTRUCTIONS

When the SD112-H is used in a mechanical impedance measuring system, it is normally mounted in the system rack. Output and input connections are made via AUX FUNCTIONS connectors located on the rear panel. (See Figure 1-3 in Section I, and schematic DWG. NO. 10928 located at the back of this manual for wiring information.) Except for the interconnection instructions, the turn-on and measuring procedures described in Paragraphs 2.3 through 2.4.4 are applicable.

NOTE

The null point of the SD112-H is 45 mV.
When interconnected with a Model SD101B

(Cont'd)

Dynamic Analyzer, set the RANGE control on the analyzer in the .1 position and the indication to its signal input meter should be approximately 45 mV.

2.5.1 Using External Filter

CONSTANT AMPLITUDE INPUT/OUTPUT connectors are provided on the rear panel for each channel. (See Figure 1-3.) For interconnection and operational information, refer to paragraph 3.4.7 in this manual and also to Instruction Manual for SD1002 Automatic Mechanical Impedance Measuring System.

The SD112-H provides stable operation for bandwidths of 2 to 200 Hz, as determined by the setting of the RESPONSE switch. For a filter bandwidth between 2 to 10 Hz, 10 to 20 Hz, or 20 to 200 Hz, set the RESPONSE switch to SLOW, MED or FAST respectively. If a filter bandwidth less than 2 Hz is desired, connect a 4 μf capacitor (Elpac ZD5A405 or equivalent) in parallel with both A3C1 (Channel 1) and A3C6 (Channel 2).

2.5.2 Mass Cancellation

It is often desirable to cancel the effects caused by the mass of the transducer (or impedance head) used in mechanical impedance instrumentation. Mass cancellation is facilitated by the SD112 when used in conjunction with an external amplifier/inverter, interconnected via rear panel connectors J1 and J11, ACCEL MASS CANCELLATION OUTPUT and FORCE MASS CANCELLATION INPUT respectively. Refer to paragraph 3.4.2.1 and Figure 3-3 in Section III of this manual.

2.6 APPLICATIONS

The following paragraphs describe typical applications in which the SD112-H provides measurement and log conversion of audio frequency signals.

2.6.1 Transfer Function Analysis

A complete description of the transfer function between two points on a specimen under test requires the recording of both magnitude and phase relationships between the two points of interest, over a specified frequency spectrum. Figure 2-1 shows the SD112-H in a transfer function analysis system.

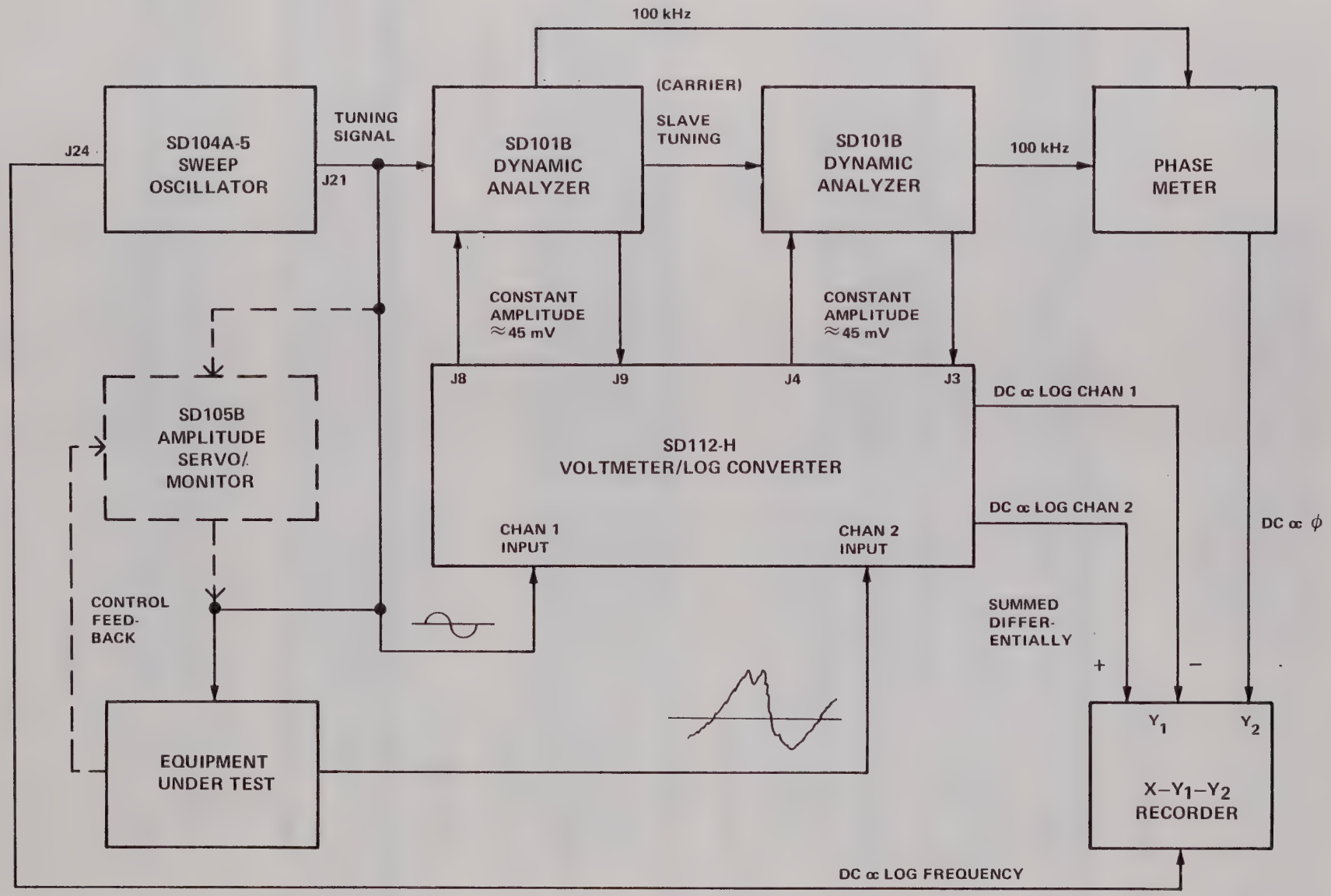


Figure 2-1. Transfer Function Analysis System

The transfer function between fundamental forcing frequency components only (with all noise, distortion, and nonlinear harmonics removed) is assured by using SD101B Dynamic Analyzers (tracking filters). The analyzers are inserted in the SD112-H servo loops. (Refer to Paragraphs 3.4.7 and 3.4.8.) This technique optimizes the dynamic range of the analyzers by providing them with constant amplitude (≈45 mV rms) input and output signals, and, in turn, each analyzer provides a 100-kHz, fixed amplitude, filtered sine wave signal for phase measuring purposes. The SD112-H will provide constant amplitude signals to the analyzers throughout an 80 dB dynamic excursion of the Channel 1 and/or Channel 2 inputs.

The Channel 1 and 2 LOG DC OUT voltages are summed differentially to produce a Y plot of the ratio of the two inputs; i.e., $\log \frac{\text{Channel 1}}{\text{Channel 2}}$.

2.6.2 Mechanical Impedance Analysis

Mechanical impedance is defined as the ratio of the force applied to a mechanical system and its resultant motion (usually velocity). Figure 2-2 is a block diagram of a system for measuring this specialized type of transfer function.

When accelerometers are used as response transducers, single integration of their outputs is required to compute mechanical impedance (Force/Velocity); double integration is required to compute dynamic stiffness (Force/Displacement).

Because electronic integration limits dynamic range, a technique called "artificial integration" has been developed. This technique, defined for sinusoidal motion only, requires the linear combination of the d-c voltage proportional to log frequency with the d-c voltage proportional to log acceleration. The SD112-H continuously supplies a d-c voltage proportional to log acceleration.

In a mechanical impedance system, the SD112-H facilitates cancelling the effects caused by the mass of the impedance head and fixture. This technique is described in Paragraph 3.4.2.1 in Section III.

2.6.3 Transmissibility and Systems Response Plotting

Many times during a sinusoidal sweep or resonant survey vibration test performed on a large specimen, several channels of response data are recorded on magnetic tape. If the transmissibility between several points on a package are required, the test configuration of Figure 2-1, either with or without the use of tracking filters, can be employed.

For test specifications which require the plotting of fundamental response amplitudes, the configuration of Figure 2-1 can also be used except that the log outputs for each individual track

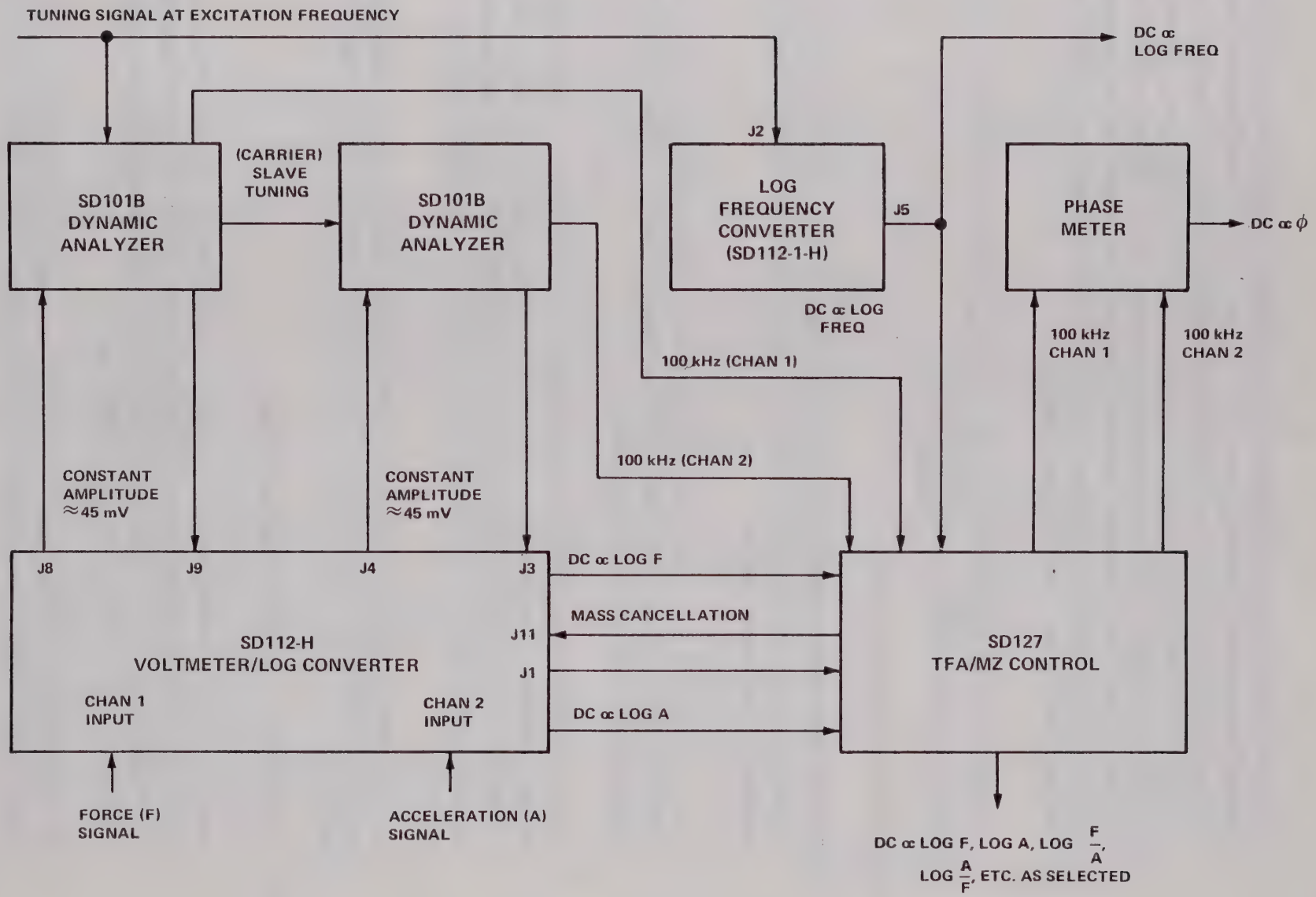


Figure 2-2. Mechanical Impedance Analysis System

are recorded separately and not in differential fashion as shown in Figure 2-1. This particular test configuration permits the recording of an extremely wide range of specimen dynamic response or dynamic transmissibility ratio.

2.6.4 Random Signal Analysis

The analysis of random signals normally involves a filtering and averaging process followed by log conversion suitable for X-Y recording and display. Figure 2-3 shows an SD112-H providing log conversion for two channels of such a system. For general random signal analysis, the a-c filtered signal output from a Dynamic Analyzer, Model SD101B is applied to the input (a-c mode) of the SD112-H. In this mode, three selectable averaging times or a-c response speeds (SLOW, MED, FAST) are available at the front panel of the SD112-H. For even the narrowest filter bandwidth in use, a steady averaged meter display and X-Y recorder output are furnished by both channels of the SD112-H.

If a specific or adjustable averaging time must be furnished, the averaged d-c output of the SD101B can be applied directly to the SD112-H d-c input. The SD112-H then produces a negligible additional averaging time constant of approximately 0.1 seconds on the log d-c output.

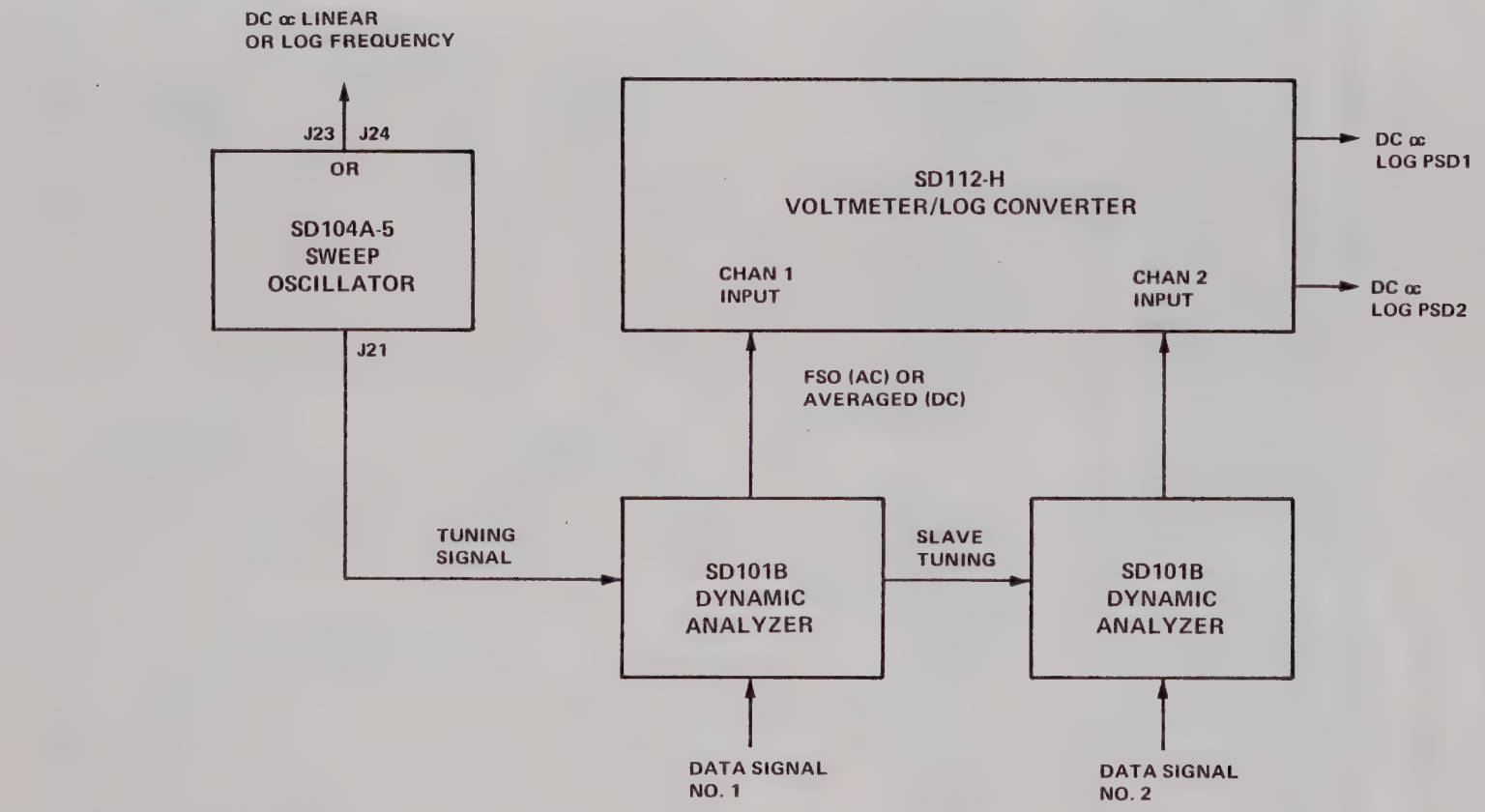


Figure 2-3. Random Signal Analysis System

SECTION III

CONCEPT AND THEORY OF OPERATION

3.1 INTRODUCTION

This section describes the concept and theory of operation of the Model SD112-H Voltmeter/Log Converter. Because both channels of the SD112-H operate the same, only the operation of Channel 1 is described.

3.2 CONCEPT OF OPERATION

The SD112-H rms voltmeter and log converter circuit utilizes the accurate nonlinear characteristic of a transdiode to provide a logarithmic conversion of the input signals. (See Figure 3-1.) In the d-c mode, a d-c input is directly converted to its d-c logarithmic equivalent, which is displayed on a front panel meter and is provided at the output terminals. In the a-c mode, the ac passes through the log converter circuit and adder, is rectified, amplified, and integrated, and after inversion is fed back to the log converter input in the form of a d-c control voltage. This d-c voltage is proportional to the rms value of the a-c input. It is converted to its logarithmic equivalent which is displayed on a front panel meter and provided at the output terminals.

3.3 BLOCK DIAGRAM DISCUSSION (See Figure 3-1.)

3.3.1 D-C Mode

In the d-c mode, R3 is grounded; therefore, the d-c voltage applied to RI controls the current flow into the log converter. The log converter is basically an operational amplifier with its gain controlled by a transdiode. Because of the nonlinear characteristics of the transdiode, the current flowing through it develops a new voltage that is proportional to the logarithm of the input voltage. This voltage is displayed on front panel meter M1, and is routed to front panel LOG DC OUTPUT connector and rear panel AUX FUNCTIONS connector.

3.3.2 A-C Mode

In the a-c mode, R3 is connected to the output of the inverter. (See Figure 3-1.) The log converter is now part of an electronic servo loop, and its gain is controlled by the current developed from the d-c feedback voltage impressed across R3. Basically, this d-c voltage is derived from the a-c input that is applied through R2 to the log converter servo loop and subsequently rectified.

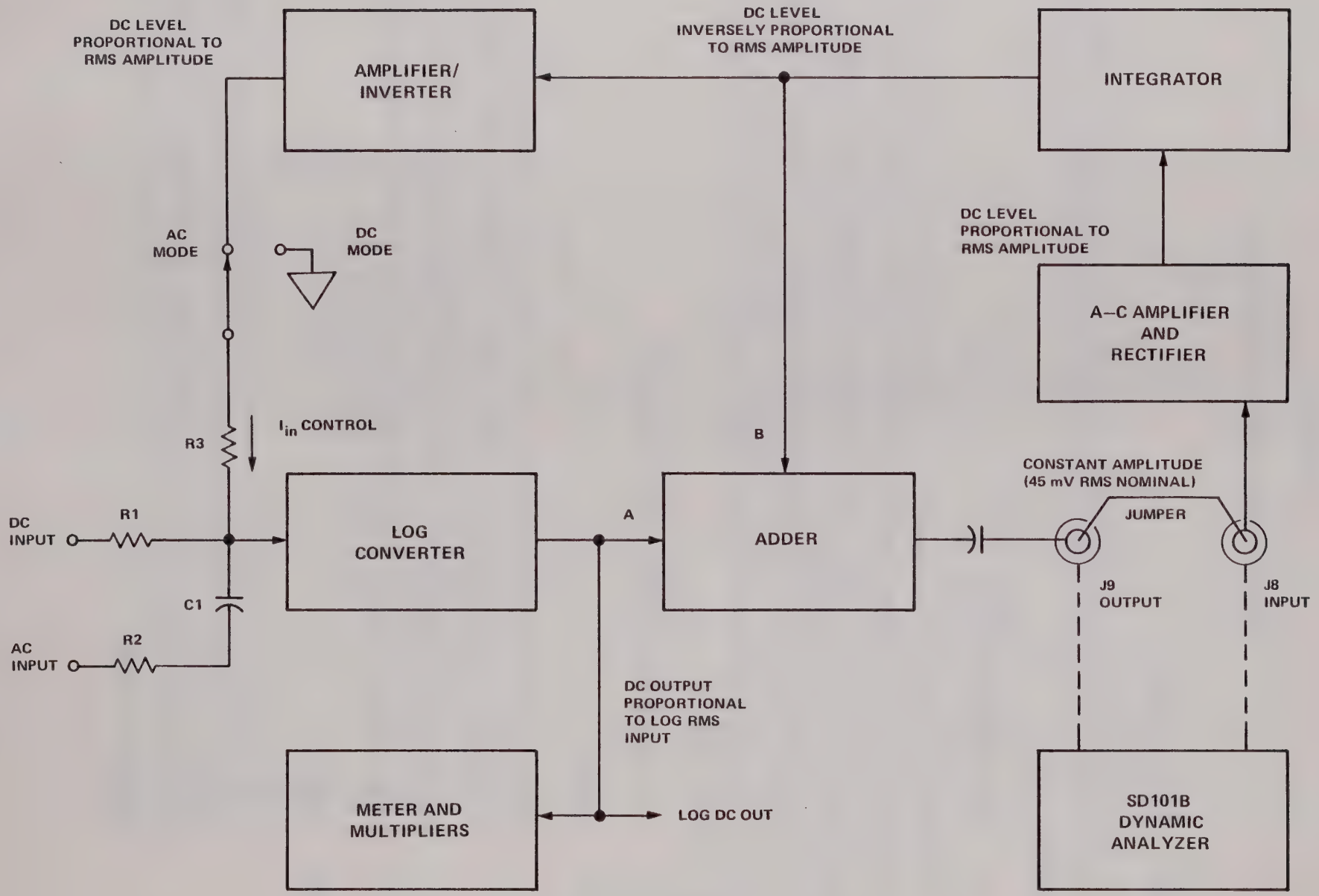


Figure 3-1. Simplified Functional Block Diagram (Channel 1)

Assume a small a-c signal is applied to the input of the log converter via R2 and C1. The a-c component passes through the adder and C2, and is then amplified and detected (rectified). This rectified +d-c voltage proportional to the rms amplitude of the a-c input, is applied to the integrator. The integrator output charges to a d-c voltage proportional to its input. This integrator output is inverted and impressed across R3 to develop the control current that drives the log converter.

Note that the d-c control voltage fed to R3 is proportional to the rms value of the a-c input; hence, the d-c control current produces a d-c voltage at the log converter output that is proportional to the log of the rms value of the a-c input. As in the d-c mode previously described, the log converter output is applied to the meter and output connectors.

If the a-c input signal level does not change, the loop signal (ac) applied through C2 remains constant at 45 mV rms nominal; the detector output remains constant thus holding the integrator output at some constant value. In this condition, the current through R3 cannot change, so the log converter output is held at the previously developed level.

Note here that the purpose of the adder is to pass only a-c signals. Its operation is as follows: When the log converter input experiences a signal level change, the two inputs (A and B) of the adder receive opposite-going d-c voltage ramps which effectively cancel each other. Therefore, only the a-c component on the input at point A passes through.

Assume now that the a-c input level is increased to some new value. As the a-c input starts to increase, the a-c level increases at the input to the adder (point A). Also, this level increase is routed through C2, amplified, and rectified. The higher value of dc applied to the integrator causes its output to integrate down. This negative-going ramp is inverted and causes an increase in the control current through R3. Because this control current is forced through a transdiode which in turn controls the log converter gain, the gain of the log converter starts to decrease logarithmically. As the a-c input approaches this higher level, the decreasing gain of the operational amplifier tends to return the loop signal to 45 mV rms. When the new level is reached, the loop stabilizes, the integrator output voltage has increased, and thus the control current supplied to the log converter is higher. Again the d-c output from the log converter is proportional to the log of the rms value of the a-c input.

3.4 THEORY OF OPERATION

Throughout the following description, refer to Figure 3-2, Functional Block Diagram of SD112-H Voltmeter/Log Converter, and to schematic DWG. NO. 10928 located at the back of this manual. Parts are referenced by their board number, and their alphanumeric designation; i.e., R4 on board A1, the

buffer/log converter board, is referred to as A1R4. The integrated circuit elements are preceded by the word "element"; i.e., the transdiode element on board A1 is designated "element A1A4". Parts mounted on the chassis, panels, and between boards are referenced by their alphanumeric part designation only.

Both Channels 1 and 2 operate in the same manner; therefore, only the operation of Channel 1 is described.

3.4.1 Input Ranging

The input signal is applied to front panel INPUT connector J15 or terminal 1 of J12, AUX FUNCTIONS connector on the rear panel, and routed to INPUT RANGE switch S1.

The three input ranges 1, 10 and 100V ac or dc are provided by the action of S1C-W1 and S1C-W2, and associated attenuator resistors R1, R2 and R3. In the a-c mode, C3 blocks any d-c voltage level that might be present in the signal.

3.4.2 Input Buffer Amplifier

Buffer amplifier (element A1A1) provides impedance isolation between the input circuitry and the log converter; its gain is unity. Input limiting is provided by A1CR1, −CR2, −CR3 and −CR4. Zener diodes A1Q1 and A1Q2 set the limiting threshold reference point. Applying voltage from the amplifier output (terminal 5) to the input limiting circuit (junctions of A1CR1, −CR2 and A1CR3, −CR4) causes the limiting circuit to present an extremely high impedance to the input signal until the point of limiting, thereby preventing leakage currents during normal signal application. This technique is called "bootstrapping".

The output signal is routed through A1-M to S1B-W2. In the a-c mode, the signal is coupled through C7, A1-K, and A1R16 to the log converter input. In the d-c mode, the signal is fed through A1-F, −R62 and −R14 to the log converter. During instrument calibration, A1R62 is used to normalize d-c linearity to a-c operation.

Amplifier element A1A1 is contained in an oven, self-stabilized at 80°C. The oven temperature stabilizing element provides a minimum temperature gain of 10; i.e., reduces ambient temperature fluctuations by a factor of 10.

3.4.2.1 Mass Cancellation

When the SD112-H is used in a mechanical impedance measuring system, the effects caused by the mass of the impedance head and fixture can be cancelled as described below.

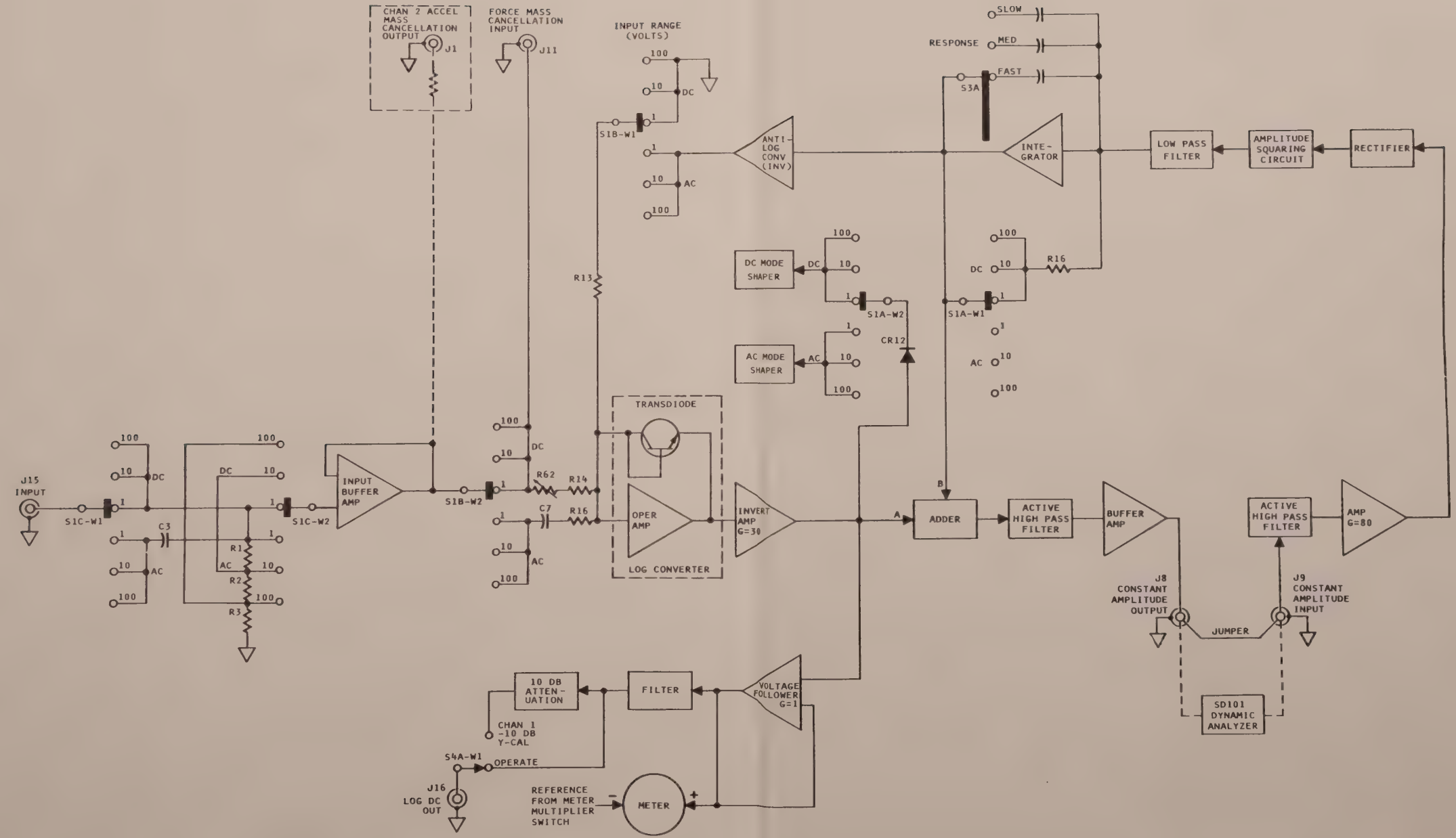
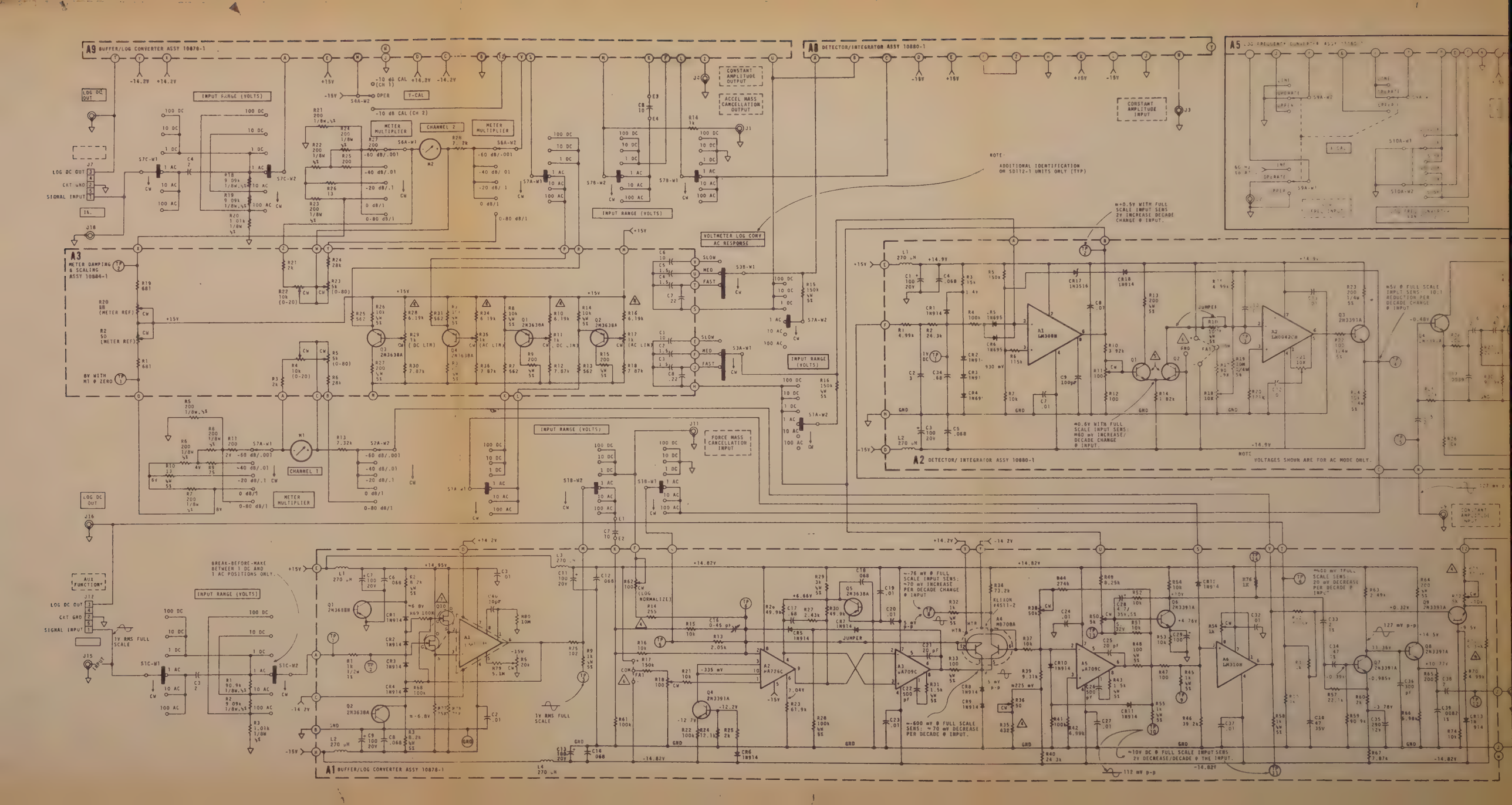


Figure 3-2. Detailed Functional Block Diagram (Channel 1)

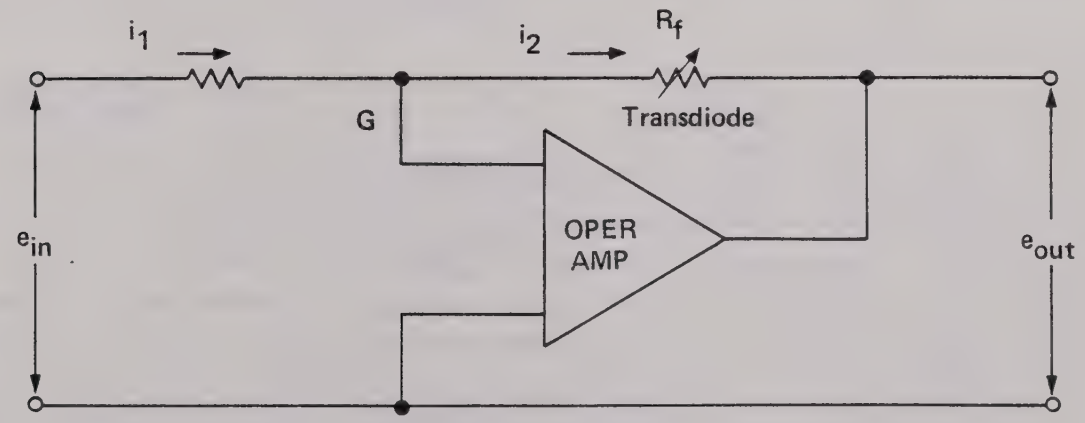

A9 BUFFER/LOG CONVERTER ASSY 10878-1
A8 DETECTOR/INTEGRATOR ASSY 10880-1
A5
A3
METER DAMPING & SCALING ASSY 10884-1
A2 DETECTOR/ INTEGRATOR ASSY 10880-1
A1 BUFFER/LOG CONVERTER ASSY 10878-1
LOG DC OUT
CKT GND
SIGNAL INPUT
INPUT RANGE (VOLTS)
METER MULTIPLIER
CHANNEL 2
CHANNEL 1
T-CAL
CONSTANT AMPLITUDE OUTPUT
ACCEL MASS CANCELLATION OUTPUT
CONSTANT AMPLITUDE INPUT
FORCE MASS CANCELLATION INPUT
VOLTMETER LOG CONV AC RESPONSE
SLOW
MED
FAST
AUX FUNCTIONS
BREAK-BEFORE-MAKE BETWEEN 1 DC AND 1 AC POSITIONS ONLY.
ADDITIONAL IDENTIFICATION ON 5D12-1 UNITS ONLY (TYP)
VOLTAGES SHOWN ARE FOR AC MODE ONLY.
1V RMS FULL SCALE
8V WITH M1 @ ZERO
0-80 dB/1
-10 dB CAL (CH 1)
-10 dB CAL (CH 2)

As shown in Figure 3-3, the outputs from the force gage and accelerometer in the impedance head are applied to Channels 1 and 2 respectively of the SD112-H. The impedance head with fixture attached is first driven without the specimen. The acceleration signal is sampled (in Channel 2 only) at the output of input buffer amplifier element A9A1 and routed through A9-M and R14 to J1, ACCEL MASS CANCELLATION OUTPUT. This signal is amplified and inverted by an external amplifier. The amplifier output is routed to J11, FORCE MASS CANCELLATION INPUT (Channel 1 only). Here it is summed with the force signal at the input of the log converter. The external amplifier null (gain) potentiometer is adjusted for a null indicated by the Channel 1 meter. This action reduces the apparent mass of the impedance head and fixture to zero. Then the specimen is attached and driven. The outputs of the SD112-H are now indicative of the specimen only.

3.4.3 Log Converter

The log converter comprises operational amplifier (elements A1A2 and A1A3), a transdiode (element A1A4), and associated circuitry.

Elements A1A2 and A1A3 operate as a conventional operational amplifier except that the overall gain is controlled by the feedback through transdiode element A1A4. Because the impedance of a transdiode varies inversely and logarithmically as the current forced through it, the overall gain of the operational amplifier is caused to vary inversely and logarithmically. Therefore, because the gain of an operational amplifier is equal to the feedback impedance divided by the input impedance ($\text{gain} = \frac{R_{FB}}{R_{IN}}$), and the transdiode impedance is varying inversely and logarithmically to the input, the voltage developed at the output is proportional to the log of the input. This function is illustrated as follows:



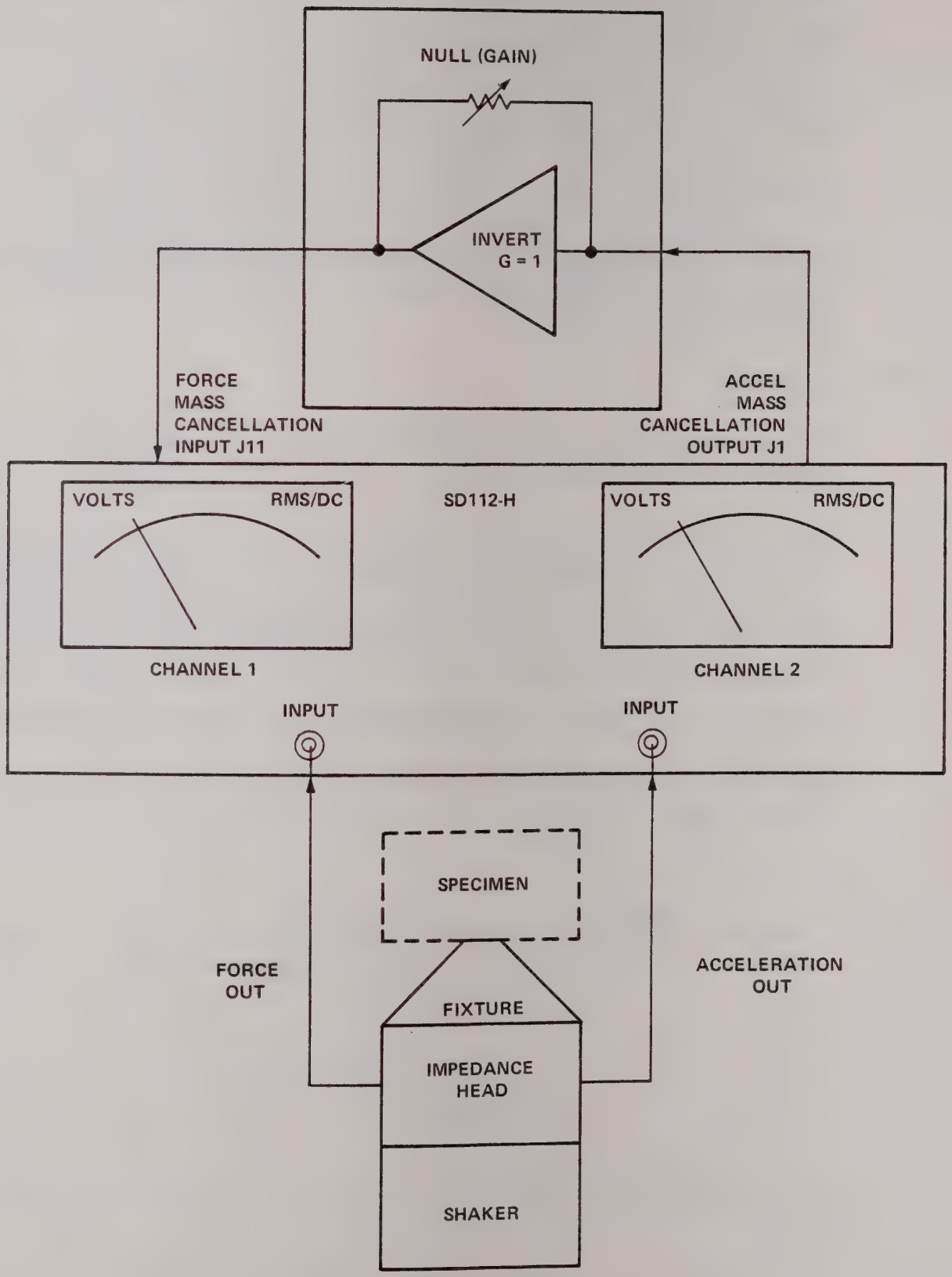


Figure 3-3. Mass Cancellation Setup

Elements A1A2 and A1A3 operate as a conventional operational amplifier with a transdiode substituted for R_f. Therefore, to maintain virtual ground at the summing junction (point G), the input current (i_1 must equal the output current (i_2). Because R_f is a transdiode (whose impedance varies logarithmically as the current passed through it), i_2 (= i_1) is proportional to the antilog of e_{out}. Also, because $i_2 = i_1 = e_{in}/R_{in}$, e_{in} is proportional to the antilog of e_{out}; or e_{out} is proportional to the log of e_{in}. This logic is given in brief mathematical form as follows:

$$i_2 \propto \exp e_{out}$$

or $$e_{out} \propto \log i_2$$ (from basic diode equation, neglecting temperature changes)

but $$i_2 = i_1 = e_{in}/R_{in}$$

therefore $$e_{out} \propto \log e_{in}/R_{in} \propto \log e_{in}$$

or $$e_{out} \propto \log e_{in}$$

The transdiode element A1A4 is contained in an oven, self-stabilized at 80°C with a minimum temperature gain of 10. This provides a stable logarithmic output characteristic curve with wide changes in ambient temperature.

Note that in the d-c mode the log converter output is applied directly to the log d-c output circuit. In the a-c mode, the log converter output is a composite signal consisting of the log d-c output and the a-c loop signal voltage. The output of the log converter is amplified (gain = 30) and inverted by amplifier element A1A5. The output of element A1A5 is routed to the output, the meter circuits, and to the servo loop.

3.4.4 Output and Meter Circuits

Amplifier element A1A6 operates as a voltage follower to provide isolation between the servo loop circuitry (output of log converter) and the output and meter circuits. A shaping circuit at the input of amplifier element A1A6 compensates for emitter-contact and base-spreading resistance of the transdiode at high currents, to maintain true logarithmic output. This circuit comprises A1CR12, A3Q1, A3Q2, and associated circuitry. In the d-c mode, A3Q1 and potentiometer A3R11 set the reference voltage level for the conduction of A1CR12; in the a-c mode A3Q2 and potentiometer A3R17 set the reference level.

The output of element A1A6 is filtered by A1R12, A1C10 and A1R11, −R10. The filtered d-c output is routed through A1-T to LOG DC OUT connector J16 on the front panel and pin 3 of J12 AUX FUNCTIONS connector on the rear panel.

3.4.4.1 Y-CAL Circuit

A calibrated −10 dB (−10 mV) can be inserted in the LOG DC OUT at this point by action of the Y-CAL switch. The Y-CAL circuit comprises S4A-W1, A1Q9, calibration potentiometer A1R72, and associated circuitry. When Y-CAL is set to CHAN 1 −10 dB, −15V is applied through A1R73 and A1R72 to emitter of A1Q9. A1Q9 draws additional current through A1R10 and A1R11, developing a −100 mV offset voltage. Because the output sensitivity is 10 mV/dB, this represents a −10 dB attenuation.

3.4.4.2 Meter Circuit

The output of element A1A6 is also routed through A1-V to S2A-W2, wiper 2 of METER MULTIPLIER switch S2A. In the 0-80 dB position, the meter is referenced to only a small voltage developed across R5; thus, the 80 dB scale is read directly and represents the voltage level in dB of the signal at the input terminals. When S2A is set to any other position, the proper reference voltage is selected by S2A-W1, which determines both the multiplier factor used with the RMS/DC meter scale (top scale) and the dB reference to be algebraically added to the −20 dB scale (center scale). (Refer to Figure 1-2 in Section I of this manual for details concerning the operation of the METER MULTIPLIER switch.)

3.4.5 Adder

The input of adder amplifier A1Q6 consists of resistive adder network A1R49, −R50, and −R51. Refer to Figure 3-2 and DWG. NO. 10928. Adder input point A on Figure 3-2 is at the junction of A1R48, −R47 and −R51. The output of element A1A5 is combined with the integrator output (point B, output of element A2A1), and the resulting a-c signal is amplified by A1Q6. Note here that in the a-c mode, the output of the integrator is a d-c voltage; its polarity is opposite to the d-c output of the log converter. Therefore, these two d-c levels effectively cancel each other; and only the ac component is amplified by A1Q6. The output of A1Q6 is fed to active high-pass filter A1Q7.

3.4.6 Active High-Pass Filter

This filter circuit comprises A1C33, −R57, −C34, −R59, −R60, −C35, and amplifier A1Q7. This circuit rejects any low frequency components that might be present at the adder output.

3.4.7 Buffer Amplifier

Amplifier A1Q8 operates as an emitter-follower, providing an impedance match between the high-Z filter and coaxial output at J8. When the instrument is used as a broadband rms voltmeter/log converter, the servo loop must be closed by a coaxial jumper between CONSTANT AMPLITUDE INPUT/OUTPUT connectors J8 and J9. (A jumper is supplied with the instrument.) When used in a system where an SD101B Dynamic Analyzer is used as a tracking filter, the proper impedance match for coaxial cabling and sufficient drive are present at J8.

3.4.8 Active High-Pass Filter and Clipper

The CONSTANT AMPLITUDE INPUT applied to J9 is buffered by A2Q4 and filtered by an active high-pass filter consisting of A2C16, -R27, -C18, -R30 and -Q5. This filter further eliminates any low frequency components that may be present in the constant amplitude loop signal. A2Q5 provides a voltage gain of about 4. The output of A2Q5 is coupled through emitter-follower A2Q6 to a clipper circuit (A2CR7, -CR8, -CR9, and -CR10). This clipper prevents excessive input to the rectifier circuit by clipping all signals greater than about 2V p-p.

3.4.9 Rectifier

Transistors A2Q7 and -Q8 operate as a differential amplifier (gain = 20) to provide two outputs, 180 degrees out-of-phase with each other, for subsequent full-wave rectification by element A2A3. A2CR11 and -CR12 provide negative peak clipping at the inputs to element A2A3. The rectified output is present at A2TP9 and is fed to the amplitude squaring circuit.

3.4.10 Amplitude Squaring Circuit

This circuit attenuates low level signals and emphasizes the passing of high level or peak signals; it thereby tends to square the amplitude of the applied d-c voltage ramp.

Low level signals are attenuated by A2R56. As the input level increases, a diode-connected transistor in element A2A4 shunts the signal through A2R57. At peak signal levels, both diode-connected transistors in element A2A4 conduct and shunt the signal directly through to buffer amplifier element A2A5. Amplifier element A2A5 provides a gain of about 7 and buffering action to drive the low-pass filter at the input to the integrator.

3.4.11 Low-Pass Filter

The low-pass filter consists of A2R1, -C2, -R2, and -C34. This double-pole low-pass filter provides a 12 dB per octave roll-off, eliminates ripple and noise, and passes only the d-c ramp voltage to activate the integrator.

3.4.12 Integrator

The integrator comprises amplifier element A2A1, storage capacitors A3C1, −C2, −C3 and −C8 selected by RESPONSE switch S3A-W1, and associated circuitry. Because the integrator is not used in the d-c mode, the storage capacitors are discharged through the contacts of S1A-W1 and R16. The integrator is quiescent until the loop signal level changes; then it operates to change the level of voltage stored in the storage capacitors.

The diode network of A2CR1, −CR12, −CR3 and −CR4 limits the positive-going ramps to about 2V peak. This action provides equal response time to both increasing and decreasing input signal ramps.

Diodes A2CR5 and −CR6 establish the input threshold level and prevent amplifier element A2A1 from responding to other than large signal changes. Small noise and ripple voltages are rejected, thereby making the integrator stable.

The output of the integrator is present at test point A2TP2, is routed through A2-B to A1-U, point B of the adder (refer to paragraph 3.4.5), and is buffered through emitter follower A2Q1 to the antilog converter (inverter).

3.4.13 Antilog Converter (Inverter)

This circuit consists of transistor A2Q2, operational amplifier element A2A2 and A2Q3, and associated circuitry. A2Q2 operates as a grounded-base current amplifier to control the d-c input drive current to operational amplifier, element A2A2 and A2Q3. This causes the gain of the circuit to vary directly as the input current; hence the voltage developed at the output of element A2A2 and A2Q3 is the antilog of the input voltage that controls A2Q2. Antilog conversion provides equal response time for any given amplitude excursion of the input signals being measured and converted by the instrument.

The output of the antilog converter is applied to A2TP4, and routed through A2-C, the a-c mode contacts of S1B-W1, and A1-L to the input of the log converter operational amplifier (elements A1A2 and −A3). The output of this circuit provides the d-c control current for transdiode element A1A4 during the a-c mode of operation.

3.4.14 Power Supply

Power supply board A7, supplied by transformer T1, provides all circuit d-c operating voltages (±15V). It also provides regulated ±14.2 volts to the oven heater circuits.

The primary power input applied at POWER IN connector J20 pin 3, is routed through fuse F1, contacts 1 and 2 of POWER switch/indicator S5, to T1 primary. The setting of switch S8 connects the T1 primary windings in parallel for 115V operation or in series for 230V operation.

Both the –15V and +15V supplies use conventional solid-state diode rectification and electronic voltage regulation circuitry. However, note that the regulation of the +15V supply is slaved to the –15V output via resistors A7R7 and A7R10. This connection causes the two supplies to track each other; i.e., their outputs, although opposite in polarity, are always equal in amplitude.

Both the +15V and –15V supply are protected against overvoltage by an SCR (silicon-controlled rectifier), a zener diode and fuse. If either output voltage tries to rise above ≈18V, voltage feedback through the zener triggers the SCR. The SCR immediately shorts the power supply output and blows the fuse.

SECTION IV

CALIBRATION AND MAINTENANCE

4.1 INTRODUCTION

This section contains calibration procedures and maintenance instructions for the Model SD112-H Voltmeter/Log Converter. The instrument has been calibrated at the factory prior to shipment and should remain calibrated indefinitely. However, because of possible amplifier gain changes over long periods of operation, and when parts are replaced, the calibration should be checked periodically and adjustments made as necessary in accordance with the procedure of Paragraph 4.2. Figure 4-1 shows a top view of the SD112-H chassis and locations of the calibration controls used with the periodic calibration procedure.

The troubleshooting procedures given in paragraph 4.3 and associated Table 4-2 are not intended to provide a remedy for every trouble that may occur. However, based on loss of meter indication and/or log d-c output voltage, the sequence of steps leads the service technician to the faulty circuit. Then, using standard circuit troubleshooting techniques along with the voltages and waveforms on the schematic, the faulty part can be isolated and repaired.

Table 4-1 lists the test equipment required to perform the periodic calibration procedure. For normal troubleshooting, only the attenuator set, digital voltmeter, volt-ohmmeter, low frequency oscillator, and oscilloscope are needed.

Table 4-1. Test Equipment Required for Periodic Calibration

Name	Model No.	Manufacturer
Attenuator Set	350D	Hewlett-Packard
*Decade Divider	Dekavider Model 412	Electro Scientific Industries
Digital Voltmeter	3440A	Hewlett-Packard
DC Power Supply	T50-2	Tryon Electronics
*Low Frequency Oscillator	202C	Hewlett-Packard
Oscilloscope	561A	Tektronix
Time Base Plug-In	Type 67	Tektronix
Wide-Band Calibrated Preamp Plug-In	Type 3A6	Tektronix
RMS Voltmeter	3400A	Hewlett-Packard
*Ratio Transformer	RT-60	Gertsch
Volt-Ohmmeter	269	Simpson
**Voltage Calibrator	738BR	Hewlett-Packard

**The HP738BR replaces the three instruments marked with an asterisk.

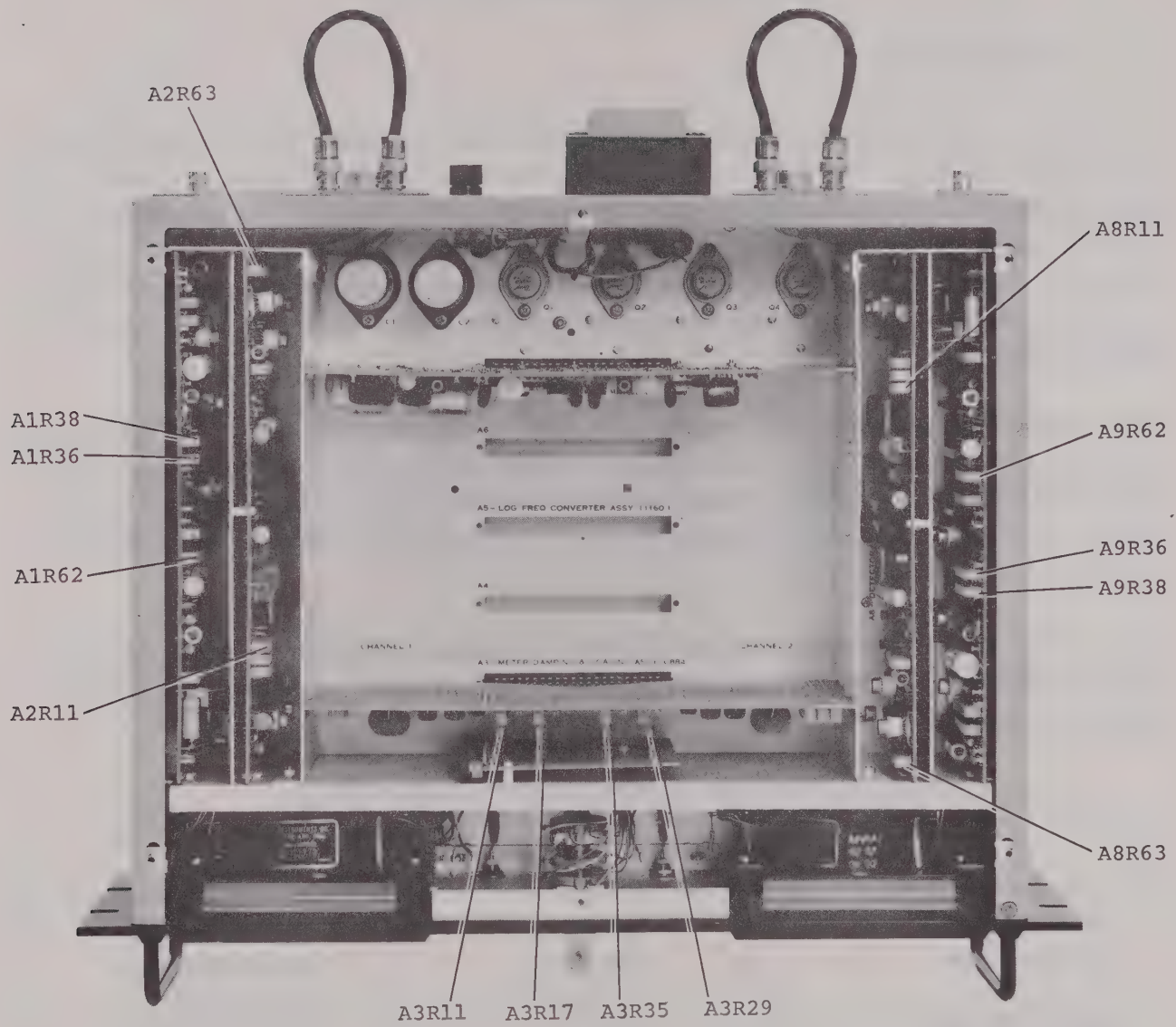


Figure 4-1. Top Chassis View — Periodic Calibration Controls

Before calibrating or troubleshooting the instrument, the technician is advised to study carefully the theory of operation in Section III, and Figures 1-2 and 1-3 in Section I which describe the front and rear panel controls, indicators, and connectors. See also the schematic DWG. NO. 10928 and its associated Circuit Card Component Identification drawing; both are located in the back of this manual. For parts replacement information, refer to paragraph 4.4.

A complete and detailed calibration procedure is given in paragraph 4.5. Because of its complexity, it is recommended that this procedure be performed only after major component replacement.

4.2 PERIODIC CALIBRATION PROCEDURE

Use the procedure first to calibrate Channel 1, and then Channel 2 substituting the adjustment controls, switches, etc. that are given in parenthesis. See Table 4-1 for the test equipment required.

4.2.1 Preliminary Setup

a. Set the SD112-H on the test bench and apply power. (Refer to paragraph 2.3 in Section II.) Allow at least a 30-minute warmup period.

b. Connect the SD112-H and test equipment as shown in Figure 4-2.

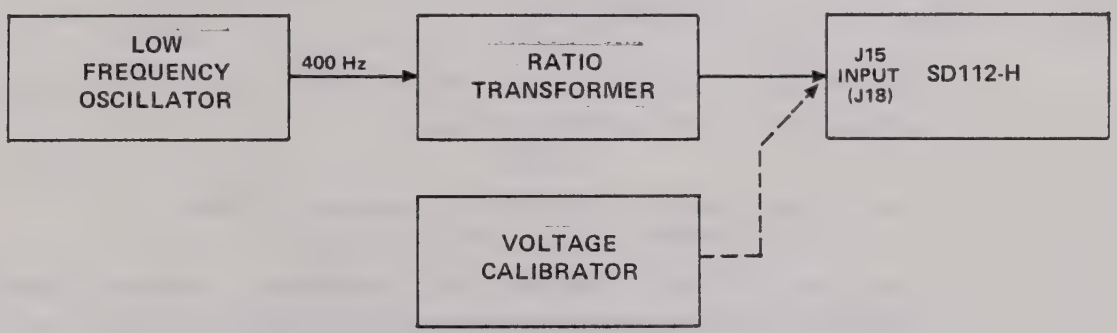


Figure 4-2. Periodic Calibration Setup, A-C Input

c. Set the SD112-H front panel controls (for both channels when applicable) as follows:

1) Set INPUT RANGE (VOLTS) switch to 1 AC.

2) Set METER MULTIPLIER switch to 0–80 dB/1.

3) Set RESPONSE switch to MED.

4) Set Y-CAL switch to OPER.

d. After warmup, remove the six screws holding the chassis top cover plate; remove the cover.

4.2.2 Servo-Loop Signal Voltage Check

NOTES

1) If an HP738BR is used as a signal source, the ratio transformer is not required, because the HP738BR provides accurately calibrated voltage levels. For example:

1V	=	0 dB
10 mV	=	-40 dB

2) Throughout the following procedures, the ratio transformer knob settings (left to right) are given in parenthesis after each attenuation value.

a. Adjust the low frequency oscillator (HP202C) for 1V ±10 mV rms output at 400 Hz monitored with the HP3400 RMS Voltmeter.

b. Adjust the ratio transformer (RT) for 0 dB attenuation (X0000).

c. Connect rms voltmeter (HP3400) and oscilloscope (Tektronix Type 561) to CONSTANT AMPLITUDE INPUT connector J9 (J3) on the SD112 rear panel.

NOTE

Ensure that a coaxial jumper is connected between J8 and J9 (J3 and J4). Use a "T" with the jumper, or connect voltmeter and oscilloscope to the connector's solder terminals inside the chassis.

d. The signal should be a clean sine wave, 45 mV ±0.5 mV rms. If not, adjust A2R63 (A8R63) for proper voltage.

e. Disconnect oscilloscope and rms voltmeter.

4.2.3 Antilog Converter Incremental Gain Check

NOTE

Test point A2TP2 (A8TP2) used for this check is located in the lower left-hand corner of board A2 (A8), just above element A2A1 (A8A1). See DWG. NO. 10928, Sheet 2. Rather than extend board A2 (A8), remove power, remove board A2 (A8), connect an insulated clip lead to A2TP2 (A8TP2), re-insert board, and reapply power.

a. Adjust the RT for −20 dB attenuation (10000).

b. Connect digital voltmeter (DVM) to A2TP2 (A8TP2) and note reading.

c. Switch RT to −40 dB (01000), and observe a 2V ±5 mV incremental change from reading of step b. If necessary, adjust A2R11 (A8R11) for a 2V ±5 mV change in DVM when RT is switched from −20 to −40 dB (10000 to 01000).

NOTE

The absolute values of the voltages are not important. Some drift is normal, however, the incremental voltage should be 2V ±5 mV each time this point is checked.

d. Remove power, remove board A2 (A8), disconnect test lead from A2TP2 (A8TP2), reinsert board, and reapply power.

4.2.4 Log Converter Incremental Gain/Normalize

NOTE

See DWG. NO. 10928 (Sheet 2) for location of test points.

a. Adjust RT for −20 dB attenuation (10000).

b. Connect DVM to A1TP11 (A9TP11) and note reading.

c. Switch RT to −40 dB (01000), and observe a 2V ± 5 mV incremental change from reading of step b. If necessary, adjust A1R38, (A9R38) for a 2V ±5 mV change on DVM when RT is switched from −20 to −40 dB (10000 to 01000).

NOTE

The absolute values of the voltages are not important. Some drift is normal, however, the incremental voltage should be 2V ±5 mV each time this point is checked.

d. With RT at −40 dB (01000), DVM should read 5.985V ±5 mV. If necessary, adjust A1R36 (A9R36) for proper voltage.

4.2.5 A-C Linearity Shaping Circuit Adjustment

a. Adjust RT for 0 dB attenuation (X0000).

b. Connect DVM to A1TP11 (A9TP11). DVM should read 10V ±25 mV. If necessary, adjust A3R17 (A3R35) for proper voltage.

4.2.6 D-C Log Normalize Adjustment

a. Connect the SD112-H and test equipment as shown in Figure 4-3.

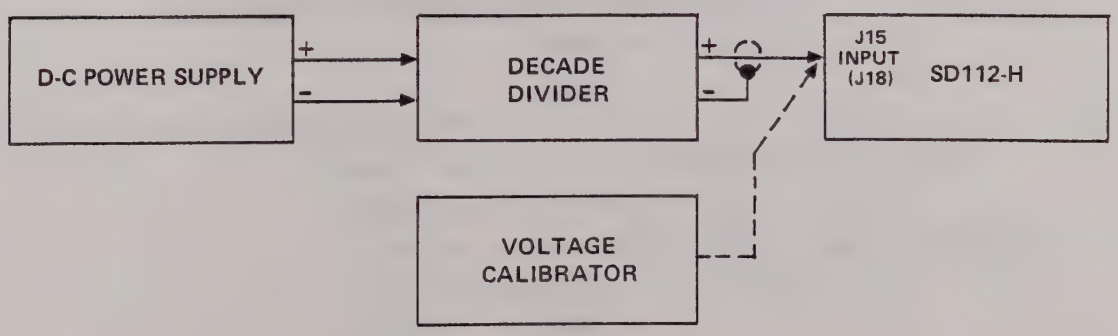


Figure 4-3. Periodic Calibration Setup, D-C Input

b. On the SD112-H, set the INPUT RANGE (VOLTS) switch to 1 DC.

c. Monitor with DVM and adjust the d-c power supply for 1V ±1 mV input to the decade divider.

d. Adjust decade divider for -40 dB attenuation.

e. Connect DVM to A1TP11 (A9TP11). DVM should read 5.985V ±5 mV. If necessary, adjust A1R62 (A9R62) for proper voltage.

4.2.7 D-C Linearity Shaping Circuit Adjustment

a. With equipment set up as shown in Figure 4-3, adjust decade divider for 0 dB attenuation.

b. DVM should read 10V ±25 mV at A1TP11 (A9TP11). If necessary, adjust A3R11 (A3R29) for proper voltage.

c. Disconnect all test equipment, replace top cover on SD112-H, and return instrument to service.

4.3 TROUBLESHOOTING

4.3.1 Introduction

A part failure will normally be indicated by the loss of meter tracking and log d-c output in either or both channels. Table 4-2 presents possible troubles and a sequence of checks that quickly isolate each trouble to a particular circuit card, circuit, or part. If the results of a check are negative, reference is made to one of the following paragraphs (4.3.2 through 4.3.5.5) which provide setup instructions and further details for troubleshooting the particular circuit.

NOTE

Each test point, part, and connector reference designator is given for Channel 1, followed by the Channel 2 reference designator in parenthesis.

The test equipment required are a digital voltmeter, an oscilloscope, a low frequency oscillator, an attenuator set, and a volt-ohmmeter. Refer to Table 4-1 for recommended models.

Table 4-2. Troubleshooting Guide

Trouble	Checkout Procedure	Action
Both channels inoperative	1. Make general checks.	Refer to paragraph 4.3.2.
	2. Check Power Supply, circuit card A7.	Refer to paragraph 4.3.3.
	3. Check all circuit cards for shorts.	Refer to paragraph 4.3.3.4.
D-C Mode inoperative (either channel)	1. Make general checks on faulty channel.	Refer to paragraph 4.3.2. If still inoperative, proceed to step 2.
	2. Prepare instrument for d-c mode bench check.	Refer to paragraph 4.3.2.1; then proceed to step 3.
	3. Connect DVM to A1TP3 (A9TP3) and read ≈1V. Switch to DC 10 and then DC 100 and read ≈0.1V and 0.01V respectively.	If voltages are correct, proceed to step 4. If not, check input buffer circuit, A1 (A9); refer to paragraph 4.3.4.1.
	4. Connect DVM to A1TP8 (A9TP8). Switch INPUT RANGE to DC 1, DC 10 and DC 100, and read ≈-75 mV, -5 mV, and +65 mV respectively.	If voltages are correct, proceed to step 5. If not, check log converter circuit A1 (A9); refer to paragraph 4.3.4.2.
	5. Connect DVM to A1TP10 (A9TP10). Switch INPUT RANGE to DC 1, DC 10, and DC 100, and read ≈10V, 8V and 6V respectively.	If voltages are correct, proceed to step 6. If not, check amplifier elements A1A5 (A9A5) and A1A6 (A9A6) and replace as necessary.
	6. Connect DVM to LOG DC OUT connector J16 (J17). Switch INPUT RANGE to DC 1, DC 10, and DC 100, and read ≈ +400 mV, +200 mV, and 0V respectively.	If voltages are correct, the d-c portion of the input buffer/log converter circuit board is operating properly; proceed to step 7. If not, check A1Q9 (A9Q9) and associated parts of the Y-CAL circuit.

Table 4-2. Troubleshooting Guide (Cont'd)

Trouble	Checkout Procedure	Action
DC Mode inoperative (either channel) (Cont'd)	7. With 1V d-c at INPUT, observe full-scale meter deflection for the following switch setting combinations: Input Range DC 1 DC 10 DC 100	If meter reads properly, proceed to step 8. If not, check the meter circuit; refer to paragraph 4.3.4.3. Meter Multiplier 0–80 dB/1 –20 dB/.1 –40 dB/.01
	8. Perform periodic calibration procedure.	Refer to paragraph 4.2.
A-C Mode inoperative (either channel)	1. Make general checks on faulty channel.	Refer to paragraph 4.3.2. If still inoperative, proceed to step 2.
	2. Prepare instrument for d-c mode bench check.	Refer to paragraph 4.3.2.1; then proceed to step 3.
	3. Connect DVM to LOG DC OUT connector J16 (J17). Switch INPUT RANGE to DC 1, DC 10, and DC 100, and read ≈ +400 mV, +200 mV, and 0V respectively.	If voltages are correct, the d-c portion of the input buffer and log converter circuits are operating properly; proceed to step 4. If not, perform steps 3. through 7. of d-c mode inoperative checkout procedure.
	4. Prepare instrument for a-c mode bench check.	Refer to paragraph 4.3.2.1. Proceed to step 5.
	5. Use oscilloscope and measure ≈3.4V p-p at A2TP7 (A8TP7) and at A2TP8 (A8TP8).	If voltages are correct, proceed to step 6. If not, check detector/integrator amplifier; refer to paragraph 4.3.5.1.
	6. Adjust oscilloscope for d-c mode, and observe correct waveform at A2TP9 (A8TP9). (See schematic DWG. NO. 10928.)	If waveform is correct, proceed to step 7. If not, check rectifier element A2A3 (A8A3) and associated circuitry; refer to paragraph 4.3.5.2.

Table 4-2. Troubleshooting Guide (Cont'd)

Trouble	Checkout Procedure	Action
A-C Mode inoperative (either channel) (Cont'd)	7. With oscilloscope in d-c mode, observe correct waveform at A2TP10 (A8TP10).	If waveform is correct, proceed to step 8. If not, check amplitude squaring circuit; replace element A2A4 (A8A4).
	8. With oscilloscope in d-c mode, observe correct waveform at A2TP11 (A8TP11).	If waveform is correct, proceed to step 9. If not, check output amplifier element A2A5 (A8A5) and associated circuitry; refer to paragraph 4.3.5.3.
	9. Connect DVM to A2TP2 (A8TP2) and measure ≈0.5V. Set attenuator to −10 dB; DVM reading should rise steadily. When DVM reads ≈9V, switch attenuator to 0 dB and observe that DVM reading decreases to ≈0.5V.	If conditions at A2TP2 (A8TP2) are correct, proceed to step 10. If not, check integrator element A2A1 (A8A1) and associated circuitry; refer to paragraph 4.3.5.4.
	10. Connect DVM to A2TP4 (A8TP4) and measure ≈5V. Set attenuator to −10 dB; DVM reading should steadily decrease. When DVM reads ≈5 mV, switch attenuator to 0 dB and observe that DVM reading increases to ≈5V.	If conditions at A2TP4 (A8TP4) are correct, proceed to step 11. If not, check antilog converter circuitry; refer to paragraph 4.3.5.5.
	11. Remove power, replace card A2 (A8) in its receptacle, and extend card A1 (A9).	Observe CAUTIONS in paragraph 4.3.2.1 a.
	Disconnect oscillator and attenuator at J9 (J3). Connect coaxial jumper between J8 and J9 (J3 and J4).	
	Apply 1 Vrms at 400 Hz to INPUT J15 (J18).	Proceed to step 12.

Table 4-2. Troubleshooting Guide (Cont'd)

Trouble	Checkout Procedure	Action
A-C Mode inoperative (either channel) (Cont'd)	12. Connect oscilloscope (a-c mode) to collector of transistor A1Q6 (A9Q6) and measure ≈112 mV p-p.	If voltage is correct, proceed to to step 14; if not, proceed to step 13.
	13. With DVM, measure voltages at A1Q6 (A9Q6). (See schematic DWG. NO. 10928.)	If voltages are correct, proceed to step 14. If not, replace A1Q6 (A9Q6) and repeat step 12.
	14. Connect oscilloscope to A1TP12 (A9TP12) and measure ≈127 mV p-p.	If voltage is correct, a-c mode is operative; perform periodic calibration procedure and return instrument to service. If voltage is incorrect, check voltages on A1Q7 (A9Q7), A1Q8 (A9Q8), and associated circuitry. Replace faulty parts and repeat step 14.

4.3.2 General Checks

Before disassembling the SD112-H for circuit troubleshooting, make the following visual checks:

a. Check all external cabling and CONSTANT AMPLITUDE jumpers (if used), and check for duplication of input signals and output loading at front and rear panel connectors.

b. Check that the 115/230 line voltage selector switch on the rear panel is set correctly, and that the applied line voltage and frequency are correct.

c. If the SD112-H is installed in a mechanical impedance system and fails to operate in the a-c mode, switch applicable dynamic analyzer to FILTER OUT. If SD112-H operates correctly, check dynamic analyzer and intercabling; if not, disconnect cables at applicable CONSTANT AMPLITUDE INPUT/OUTPUT connectors and connect coaxial jumper as shown in Figure 1-3, Section I. If a-c mode is still inoperative, refer to Table 4-2.

4.3.2.1 Bench Check Setup

a. Preliminary – Set the SD112-H on a test bench, remove the five screws holding the chassis top cover plate, and remove the cover. Note that when facing instrument front panel, all Channel 1 components (cards A1, A2 and left side of A3) are located left of center; all Channel 2 components (cards A9, A8, and right side of A3) are located right of center.

A circuit card extender assembly (23060-1) is located in receptacle A4. Whenever it is necessary to extend a circuit card, observe the following CAUTIONS:

CAUTIONS

1) Be sure power is off. Then remove circuit card, remove nylon insert from receptacle (save), insert extender card (assembly 23060-1), insert card under test on extender card with parts oriented in proper direction, then apply power.

2) After checks are completed, remove power, separate circuit card from extender card, remove extender card, replace nylon insert in receptacle (adjacent to black dot on circuit plate), and replace circuit card.

b. D-C Mode – Perform preliminary procedure a. above, and proceed as follows:

1) Remove card A1 (A9), remove nylon insert (save), insert extender card, and insert circuit card on extender card, with parts oriented in proper direction.

2) Set INPUT RANGE switch to DC 1 and METER MULTIPLIER to 0–80 dB/1.

3) Apply 1 volt d-c to input J15 (J18).

4) Apply power and allow 15-minute warmup.

c. A-C Mode – Perform preliminary procedure a. above, and proceed as follows:

1) Remove card A2 (A8), remove nylon insert (save), insert extender card, and insert circuit card on extender card, with parts oriented in proper direction.

2) If necessary, disconnect the coaxial jumper at CONSTANT AMPLITUDE INPUT connector J9 (J3) on SD112-H rear panel.

3) Connect output of low frequency oscillator to attenuator input; connect output of attenuator to J9 (J3).

4) Set attenuator to 0 dB. Adjust oscillator for output of 127 mV p-p, 400 Hz, measured at J9 (J3) with an oscilloscope.

5) Apply power to SD112-H and allow 15-minute warmup.

4.3.3 Power Supply Inoperative

4.3.3.1 Preliminary Setup

Remove the cover. Note that in this position, all power supply test points are easily accessible along the top of Power Supply Circuit Card A7. Apply power; no warmup time is required.

a. Check for proper voltages at TP1 (+14.2V), TP2 (+15V), TP3 (-15V), and TP4 (-14.2V). If no voltages are present, check a-c input circuit. If voltages are low, or only certain voltages are present, a partial short might exist. Proceed to step b.

b. Remove power, then remove all cards (A1, A2, A3, A7, A8 and A9).

c. With an ohmmeter, check for a short between pin L of receptacle XA7 and each of the following pins: XA7-R, -H, -A, and -D. If a short exists, a visual inspection should locate the problem.

d. Check for shorted capacitors on card A7:

Ohmmeter Between Pins	Capacitors Under Test
A7-L and A7-R	A7C6, A7C7
A7-L and A7-F	A7C13, A7C14
A7-K and A7-H	A7C4, A7C5
A7-K and A7-N	A7C11, A7C12

e. Check capacitors C1 and C2 on circuit plate: Measure between receptacle pins XA7-L and XA7-X (C1), and between XA7-L and XA7-M (C2).

f. Check fuses on circuit card A7; if necessary replace and go to paragraph 4.3.3.2.

4.3.3.2 Powered Checks

Place the SD112-H on its side and remove the bottom chassis cover plate. Connect a 510 ohm 5%, 1/2 watt resistor between receptacle pin XA7-K and each of the following pins: XA7-H, -D, -A, and -R. Be sure jumpers are connected between XA7-K and -D, and between XA7-Y and -CR. Return the SD112-H to its normal position and proceed as follows:

a. Remove nylon insert in receptacle XA7, insert extender card, and place card A7 on top of extender card with parts oriented properly.

NOTE

Do not insert other cards at this time.

b. Apply power; no warmup is required.

c. With voltmeter, measure rectified voltage inputs to regulator circuits: A7-L (-) to A7-M (+) ≈40V, A7-L (+) to A7-X (-) ≈ -40.5V. (See schematic DWG. NO. 10928.)

d. Check the -15V section (A7TP3) for proper voltage (-15V). Note that the -14.2V and the +15V section are slaved to the -15V bus. If the -15V section is operating, proceed to step h.; if not, proceed to step e.

e. Check all voltages on transistors Q4, A7Q9, and A7Q11. The three important check points are emitter and base of A7Q11, and collector of A7Q9 (37.7V). (A7CR7 sets reference for A7Q11, A7Q11 controls A7Q9, which in turn controls series regulator Q4.)

NOTE

If the preceding voltages are not correct, and it is suspected that the +15V section is introducing the error, isolate the two sections. Disconnect one end of both resistors A7R7 and A7R10.

After the -15V section has been checked out satisfactorily measure -14.2V at A7TP4. If voltage is correct, proceed to step g.; if not, proceed to step f.

f. Check all voltages on transistors A7Q7 and Q3. Make repairs as necessary and proceed to step g.

g. Reconnect resistors A7R7 and A7R10. Proceed to step h.

h. Check all voltages on transistors A7Q3, A7Q2, A7Q5, and A7Q4. The three important check points are emitter and base of A7Q5 and base of A7Q2. (A7Q4 only provides temperature stability for A7Q5. A7Q5 controls A7Q2 which controls series regulator A7Q3.)

i. Measure +14.2V at A7TP1. If not correct, check Q3, A7Q7, and associated circuitry.

4.3.3.3 Final Checks

a. After the power supply has been satisfactorily checked out and all output voltages are correct, remove power, remove card A7, remove extender card, and replace nylon insert and card A7 in receptacle XA7.

b. Reapply power and check proper voltages at A7TP1, A7TP2, A7TP3 and A7TP4.

c. Remove power, and disconnect the four 510 ohm resistors. Be sure jumpers are connected between XA7-W and -H, and between XA7-N and -P.

CAUTION

To ensure no damage to the power supply circuitry when other cards are inserted, perform the circuit card short test that follows in paragraph 4.3.3.4.

4.3.3.4 Circuit Card Short Test

The approximate resistances between the d-c power buses and ground on cards A1 (A9), A2 (A8), and A3 are listed as follows:

Card A1 (A9), Assembly 10878-1

Between Pins	Resistance	Between Pins	Resistance
2 and 3	> 1 MΩ	19 and 5	> 20 kΩ
2 and 4	> 1 MΩ	19 and 7	> 10 kΩ
2 and 5	> 1 MΩ	19 and 20	> 1 MΩ
2 and 7	> 50 kΩ	19 and 21	> 1 MΩ

Card A2 (A8), Assembly 10880-1

Between Pins	Resistance	Between Pins	Resistance
7 and 4	> 5 kΩ	8 and 9	>10 kΩ
7 and 5	> 10 kΩ	8 and 10	>5 kΩ

Card A3, Assembly 10884-1

Between pins 11 and 12, resistance >2kΩ.

If a short or very low resistance is found, see schematic and associated component layou drawings (DWG. NO. 10928, sheets 1 and 2). Disconnect one end of each part that ties betwee d-c power bus and ground until short is eliminated, and thus, the faulty part is found.

After all cards have been checked out satisfactorily, insert them into their proper receptacles Apply power, and again check for correct voltages at A7TP1, A7TP2, A7TP3 and A7TP4.

If all power supply voltages are correct, check SD112 overall performance (both channels) a follows:

a. Set INPUT RANGE switch to DC 1, METER MULTIPLIER to 0—80 dB/1, Y-CAL t OPER, and RESPONSE to MED.

b. Apply 1V d-c to INPUT J15 (J18) and connect DVM to LOG DC OUT J16 (J17).

c. Switch INPUT RANGE to DC 1, DC 10, and DC 100, and read ≈+400 mV, +200 mV, an 0V respectively.

d. Observe full-scale meter deflection for the following switch setting combinations:

Input Range	Meter Multiplier
DC 1	0—80 dB/1
DC 10	—20 dB/.1
DC 100	—40 dB/.01

e. Disconnect 1V d-c from INPUT J15 (J18).

f. Set INPUT RANGE to AC 1 and METER MULTIPLIER to 0—80 dB/1.

g. Apply 1 Vrms, 400 Hz, to INPUT J15 (J18).

h. Switch INPUT RANGE to AC 1, AC 10, and AC 100, and read +400 mV, +200 mV, and 0V respectively.

i. Observe full-scale meter deflection for the following switch setting combinations:

Input Range	Meter Multiplier
AC 1	0–80 dB/1
AC 10	–20 dB/.1
AC 100	–40 dB/.01

If the results of the preceeding checks are satisfactory, remove power, replace bottom and top chassis covers, and return the instrument to service.

If a fault exists in either channel for either a-c or d-c mode of operation, refer to Table 4-2 for further troubleshooting information.

4.3.4 D-C Mode Inoperative

4.3.4.1 Input Buffer

With 1V d-c applied to the INPUT, check input attenuator circuit. Connect DVM to A1TP1 (A9TP1) and switch INPUT RANGE to DC 1, DC 10, and DC 100. DVM should read ≈1V, 0.1V, and 0.01V respectively.

Visually inspect element A1A1 (A9A1) and associated parts. See the schematic DWG. NO. 10928, and check for proper voltages at pins 2 and 6 of element A1A1 (A9A1). If A1A1 (A9A1) is defective, the output will usually saturate (go to ≈+15V or –15V). Also, with oscilloscope, check for oscillations at A1TP3 (A9TP3).

Check for proper voltages on A1Q1, A1Q2, and A1Q3 (A9Q1, A9Q2, and A9Q3). Defective A1Q1 and/or A1Q2 would cause loss of overload protection for A1A1. Defective A1Q3 (A9Q3) would cause only slight nonlinearity in the output as the input signal voltage is varied.

4.3.4.2 Log Converter

The log converter circuit comprises operational amplifier [elements A1A2, A1A3 (A9A2, A9A3)], transdiode element A1A4 (A9A4), and associated circuitry. Check this circuit as follows:

a. Remove element A1A3 (A9A3) from its socket.

b. Apply 1V d-c INPUT and set INPUT RANGE to DC 1.

c. With DVM, measure and record voltages at pins 4 and 9 of element A1A2 (A9A2).

d. Switch INPUT RANGE to DC 100; the voltages at pins 4 and 9 should change by ≈300 mV from those recorded in step c. If voltages are correct proceed to step f.; if not, proceed to step e.

e. Transistor A1Q4 (A9Q4) provides a constant current source for element A1A2 (A9A2). With DVM, check for ≈6.7V at collector of A1Q5 (A9Q5); A1Q5 (A9Q5) operates as a zener regulator. Also check for proper voltages at emitter, base, and collector of A1Q4 (A9Q4). If all voltages are correct, replace element A1A2 (A9A2).

f. Reinsert element A1A3 (A9A3).

g. Remove jumper between A1TP6 (A9TP6) and pins 1, 2 of element A1A4 (A9A4).

h. Connect a 10k ohm resistor between A1TP6 (A9TP6) and pin 3 of element A1A4 (A9A4). Amplifier elements A1A2 and A1A3 are now operating as a unity gain operational amplifier.

i. Set INPUT RANGE to DC 1 and apply 1V d-c to INPUT.

j. Measure 1V d-c at pin 3 of element A1A3 (A9A3). If voltage is not correct, replace element A1A3 (A9A3). If this voltage is correct, check diodes A1CR8 and A1CR9 (A9CR8, A9CR9). If these diodes are good, replace element A1A4 (A9A4).

k. Remove 10k ohm resistor installed in step h., and replace jumper between A1TP6 (A9TP6) and pins 1, 2 of element A1A4 (A9A4).

4.3.4.3 Meter Circuit

See the schematic DWG. NO. 10928, and using DVM check that the output of element A1A6 (A9A6) is present at the METER MULTIPLIER switch S2A-W2 (S6A-W2). With the proper voltages applied to the (+) side of M1 (M2), the fault could be either M1 (M2) or the reference voltage circuit applied to the (−) side of M1 (M2). Check the meter reference voltage circuit as follows:

a. Remove power, remove card A1 (A9), and reapply power. Note that with card A1 (A9) out, no voltage is applied to (+) side of M1 (M2); hence M1 (M2) is electrically zeroed.

b. Measure 8V at A3TP1 (A3TP2). If voltage is correct, then check voltages at (−) side of M1 (M2) while switching S2 (S6) through each position. If all voltages are correct, the meter is defective.

4.3.5 A-C Mode Inoperative

4.3.5.1 Detector/Integrator Input Amplifier

a. With 127 mV, 400 Hz, applied to J9 (J3), use oscilloscope and check for proper signal at A2TP6 (A8TP6). See schematic DWG. NO. 10928. If signal is correct, proceed to step d.; if not, proceed to step b.

b. Check all d-c voltages on A2Q4, A2Q5, and A2Q6 (A8Q4, A8Q5, A8Q6). A2Q4 (A8Q4) and A2Q6 (A8Q6) are emitter followers. A2Q5 (A8Q5) is a voltage amplifier with a gain of ≈ 4.

c. Check voltage across A2C20 (A8C20). A2C20 (A8C20) bypasses A2R34 (A8R34) to maintain proper gain in A2Q5 (A8Q5) circuit.

d. Check all d-c voltages and signal voltages at A2TP7 (A8TP7) and on A2Q7 and A2Q8 (A8Q7, A8Q8). These transistors operate as a differential amplifier to amplify the difference between:

1) The signal voltage applied to base of A2Q7 (A8Q7), and

2) A fixed bias [from A2R51 (A8R51)] applied to base of A2Q8 (A8Q8).

4.3.5.2 Rectifier Element A2A3 (A8A3)

Element A2A3 (A8A3) operates as a full-wave rectifier. A2CR11 and A2CR12 (A8CR11, A8CR12) prevent large negative voltages from overloading the rectifier inputs. (This condition would cause the rectifier junctions to act as zeners.) If the waveform is not correct at A2TP9 (A8TP9), check A2CR11 and A2CR12 (A8CR11, A8CR12). If these diodes are good, replace element A2A3 (A8A3).

4.3.5.3 Output Amplifier A2A5 (A8A5)

Amplifier element A2A5 (A8A5) is connected as a conventional operational amplifier. If input is correct, adjust feedback potentiometer A2R63 (A8R63) for proper waveform at A2TP11 (A8TP11). If adjusting A2R63 does not provide correct output, check voltages at pins 4 and 7 of A2A5 (A8A5). If voltages are correct but output is still incorrect, replace element A2A5 (A8A5).

4.3.5.4 Integrator Element A2A1 (A8A1)

With 127 mV p-p, 400 Hz applied to J9 (J3), the voltage at A2TP1 (A8TP1) should be approximately 1V d-c. Attenuate the input by −10 dB, and voltage at A2TP1 (A8TP1) should drop to ≈300 mV. Return input to 127 mV p-p, and check for correct voltage at junction of A2R5, A2R6 and A2R7 (A8R5, A8R6, A8R7). Also check integrating capacitors A3C1, A3C2, A3C3 and A3C8 (A3C4, A3C5, A3C6 and A3C7). Then check diodes A2CR5 and A2CR6 (A8CR5, A8CR6). If no defect has been found to this point, replace element A2A1 (A8A1).

4.3.5.5 Antilog Converter

a. With 127 mV p-p, 400 Hz, applied to J9 (J3), use a DVM and measure −0.6V at emitters of A2Q1 and A2Q2 (A8Q1, A8Q2).

b. Attenuate input by −20 dB; DVM reading should increase ≈60 mV. If voltage change is not correct, check A2R11 (A8R11). If DVM reading is still incorrect, replace matched-pair transistors A2Q1, A2Q2 (A8Q1, A8Q2).

c. Repeat step 10. of A-C Mode Inoperative (Table 4-2). If voltages at A2TP4 (A8TP4) are still in error, check A2Q3 (A8Q3) and then element A2A2 (A8A2). Replace faulty parts as necessary.

4.4 PARTS REPLACEMENT

Except for some special SDC specification-controlled parts listed in Table 4-3, which must be ordered from Spectral Dynamics Corporation, standard electronic parts have been used throughout the instrument. Spectral Dynamics Corporation maintains a complete stock of all parts and complete printed circuit card assemblies used in this instrument.

When ordering a replacement part or assembly, be sure to include the reference designation, the part number of manufacturers designation, and a complete description; include also the instrument name, model number, and serial number.

Table 4-3. Special Replaceable Parts List

Reference Designation	Description	Part Number/ Mfr. Designation
A1	Buffer/Log Converter	10878-1
A2	Detector/Integrator	10880-1
A3	Meter Damping and Scaling	10884-1
A4	Circuit Card Extender Assembly	23060-1
A5, A6	Not used	–
A7	Power Supply	11538-1
A8	Same as A2	
A9	Same as A1	
M1, M2	Meter, Volts-RMS/DC	20013-153
A2Q1, Q2	2N3391A (Factory selected pair)	20013-044A
S1, S7	Switch, INPUT RANGE	20013-167
S2, S6	Switch, METER MULTIPLIER	20013-168
S3, S4	Switch, RESPONSE/Y-CAL	20013-166
S5/DS1	Switch/Indicator Lamp	10529000
T1	Power Transformer	20013-169
	Cable Assembly, Coaxial Jumper	11123-1
	Cord, Power	Belden 17258-S
	Knob, METER MULTIPLIER	20013-174
	Knob, INPUT RANGE	20013-175
	Knob, RESPONSE	20013-176
	Knob, Y-CAL	20013-177

4.5 DETAILED CALIBRATION PROCEDURE

This detailed calibration procedure is the procedure used by the factory during final instrument checkout and calibration. Performance of this procedure should not be attempted unless the following prerequisites are met:

a. The technician must be competent and experienced with equipment using similar circuitry.

b. All test equipment listed in Table 4-4 must be available and properly calibrated; any substitutes must exhibit operating characteristics equal to or better than the equipment listed.

Table 4-4. Test Equipment Required for Detailed Calibration

Name	Model No.	Manufacturer
Attenuator Set	350D	Hewlett-Packard
Attenuator, Switchable 0 and 40 dB	T69*	Spectral Dynamics
DVM Averager	T70**	Spectral Dynamics
Digital Voltmeter	3440A	Hewlett-Packard
Dual Trace Amplifier Plug-In	Type 72	Tektronix
Dynamic Analyzer (with 2 Hz, 10 Hz, and 20 Hz filter units)	SD101B***	Spectral Dynamics
Low Frequency Oscillator	202C	Hewlett-Packard
RMS Voltmeter	3400A	Hewlett-Packard
Storage Oscilloscope	Type 564	Tektronix
Sweep Oscillator	SD104A***	Spectral Dynamics
Time Base Plug-In	Type 2B67	Tektronix
Voltage Calibrator or	738BR	Hewlett-Packard
Ratio Transformer	RT60	Gertsch
Volt-Ohmmeter	269	Simpson

*See Figure 4-5
**See Figure 4-6
***No substitute

c. Time must be allotted so that the procedure can be performed in its entirety.

Total familiarization with the procedure and its application to the instrument can be achieved by first reading through the entire procedure while referring to the schematic diagram, DWG. NO. 10928. Figure 4-4 shows a top view of the SD112-H with cover removed exposing all calibration controls used for the detailed calibration procedure.

4.5.1 Test Equipment Required

Table 4-4 lists the test equipment required to perform the detailed calibration procedure. Except for the SD101B Dynamic Analyzer and SD104A Sweep Oscillator, test equipment exhibiting equal or better operating characteristics than the equipment listed may be substituted. The T69 Attenuator and T70 DVM Averager units can be fabricated locally; see Figures 4-5 and 4-6 respectively for circuit diagrams and construction techniques.

4.5.2 Preliminary – POWER Off

a. Mechanically adjust both front panel meters to 1 on top scale.

b. Set 115/230 volt switch on chassis rear panel to show proper input line voltage, and accordingly check for proper FUSE (115 Vac, 1A SLO BLO; 230 Vac, 1/2-A SLO BLO).

c. Remove jumper between CIRCUIT GND and CHASSIS GND on chassis rear panel, and measure resistance between binding posts. Resistance should be 2 megohms or more. Replace jumper.

d. Install coaxial jumpers between CONSTANT AMPLITUDE INPUT/OUTPUT connectors J3 and J4, and J9 and J8.

e. Set front panel controls (both channels) as follows: Y-CAL to OPER, INPUT RANGE (VOLTS) to AC 1, METER MULTIPLIER to 0–80 dB/1, RESPONSE to MED.

f. Remove the six screws holding the chassis top cover plate, and remove the cover.

4.5.3 Preliminary – POWER On

a. Apply power; red POWER switch/indicator should light. Allow a 15-minute warm-up period.

b. Connect DVM to A7TP3, and adjust A7R19 for –15V ±0.01V.

c. Connect DVM to A7TP2, and adjust A7R9 for +15V ±0.01V. Recheck step b.

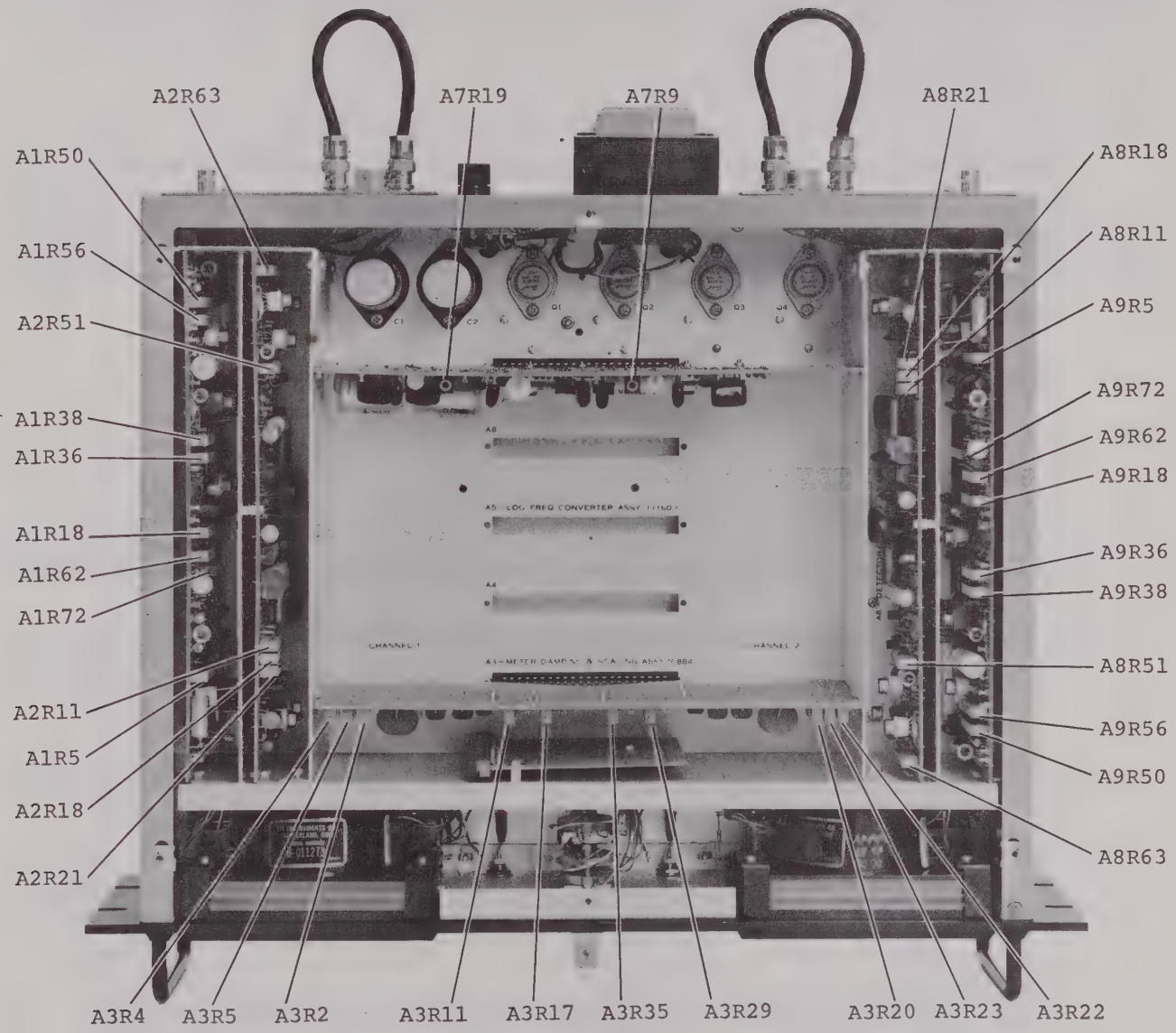


Figure 4-4. Top Chassis View — Calibration Controls (Complete)

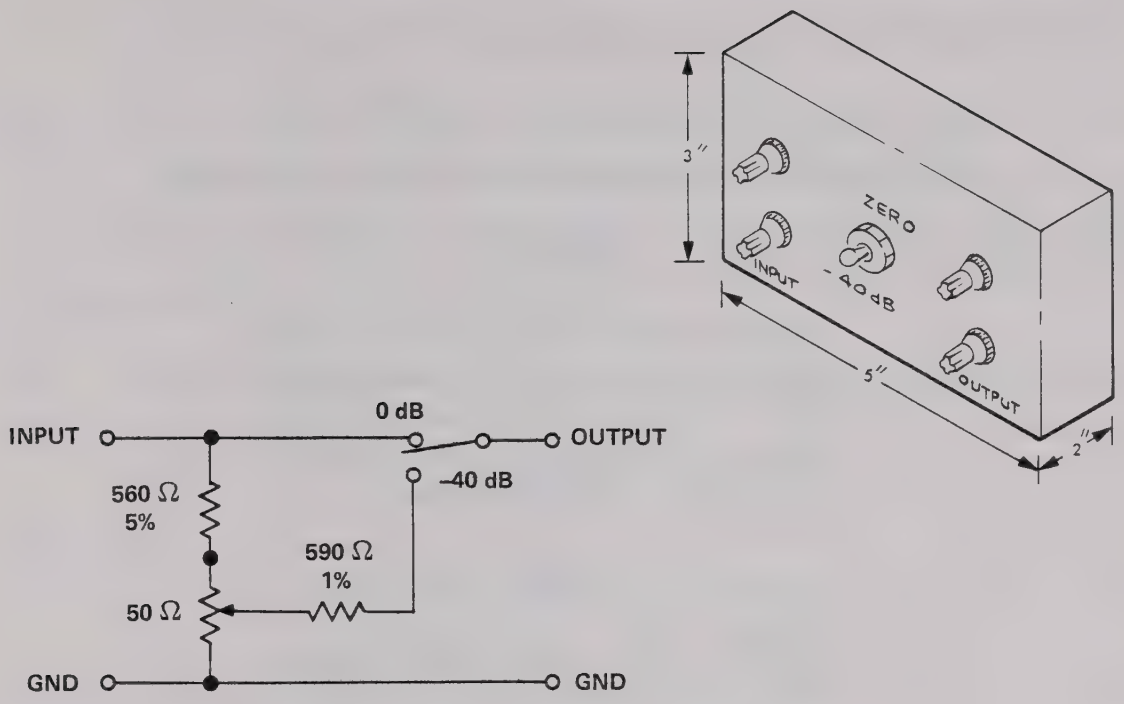


Figure 4-5. Attenuator, Switchable 0 and 40 dB (T69)

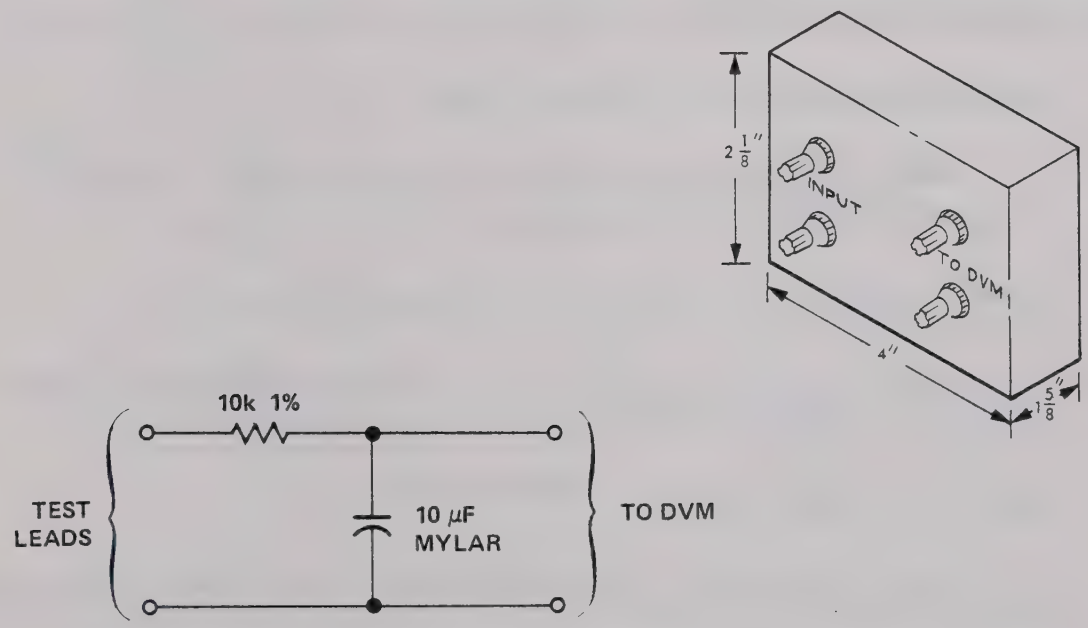


Figure 4-6. DVM Averager (T70)

d. Connect DVM to A7TP1; DVM should read +14.5V ±0.5V.

e. Connect DVM to A7TP4; DVM should read −14.5V ±0.5V.

f. Connect oscilloscope to the following test points and check for less than 2 mV p-p ripple at A7TP3 and A7TP2, and less than 20 mV p-p at A7TP1 and A7TP4.

CAUTION

Throughout the following procedure, when a printed circuit card must be extended, always remove power first. Working quickly, extend board and reapply power. Allow 3 minutes for warmup before proceeding with check.

NOTE

Paragraphs 4.5.4 through 4.5.16 calibrate Channel 1; all SD112-H connector, meter, and front panel controls referenced are CHANNEL 1.

4.5.4 Input Buffer/Log Converter (A1)

Remove power, extend board A1, and reapply power.

a. Jumper A1TP2 to ground terminal on board A1 and connect DVM to A1TP3. Adjust A1R5 for 0V ±0.1 mV. Remove jumper at A1TP2.

Set INPUT RANGE (VOLTS) switch to DC 1, and connect DVM to A1TP6.

b. Jumper terminal at top end of A1R17 to either the −15V or +15V terminal above A1R17, which gives a DVM reading of 0V ±0.1 mV as adjusted by A1R18.

4.5.5 Amplifier/Detector Calibration (A2)

Remove power, replace board A1 in its receptacle (without key), extend board A2, remove left end of jumper wire above A2R16, −R12, −R19, −R17, and connect to GND terminal below A2R16. Remove one end of jumper wire at right side of A2R16 and reapply power.

a. Connect DVM to A2TP3, and adjust A2R21 for 0V ±0.1 mV.

b. Connect DVM to A2TP4. Jumper terminal at bottom end of A2R17 to either the –15V or +15V terminal, which gives a DVM reading of 0V ±0.1 mV as adjusted by A2R18.

c. Connect DVM to A2TP3; if necessary, readjust A2R21 for 0V ±0.1 mV.

Remove power. Replace jumpers at right of A2R16 and above A2R16, –R12 etc. and reapply power. Remove coaxial jumper between CONSTANT AMPLITUDE OUTPUT/INPUT connectors J8 and J9 on chassis rear panel. On DVM, disconnect jumper between INPUT signal ground and chassis ground so DVM accepts differential input.

d. Connect DVM signal INPUT's to A2TP7 and A2TP8; adjust A2R51 for 0V ±10 mV.

NOTE

Because some noise exists at A2TP7 and A2TP8, adjust A2R51 for an average value. On DVM reconnect jumper between input signal ground and chassis ground.

4.5.6 Amplifier/Detector Operation (A2)

Install 2 Hz and 10 Hz filter units in positions 1 and 2 respectively in the SD101B. Ensure that all test equipment is warmed up and stabilized, and connect the SD112-H and test equipment as shown in Figure 4-7.

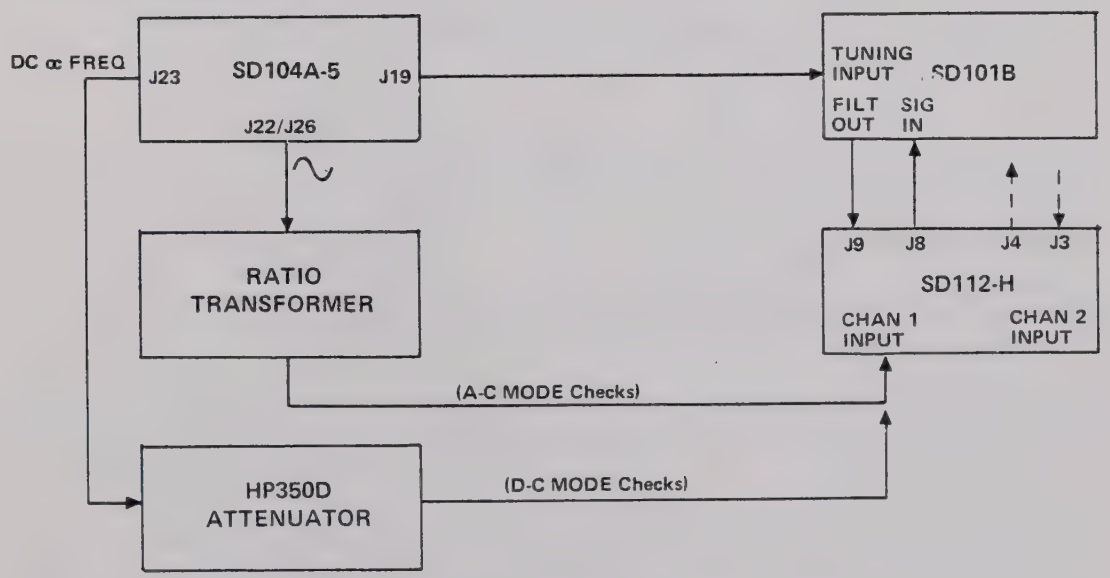


Figure 4-7. General Test Setup for Channel 1 Detailed Calibration

NOTE

Throughout the following procedures, the ratio transformer knob settings (left to right) are given in parenthesis after each attenuation value.

Set SD112-H INPUT RANGE (VOLTS) switch to AC 1. Set ratio transformer (RT) for 0 dB attenuation (X0000). Adjust the SD104A for sine wave output of 1 Vrms ±10 mV, 400 Hz, measured at SD112-H INPUT. Set SD101B RANGE switch in the .1 position and FILTER switch to OUT. Connect oscilloscope and rms voltmeter to Channel 1 CONSTANT AMPLITUDE INPUT J9.

a. Adjust A2R63 for 45 mV ±0.5 mV rms, clean sine wave at J9.

Disconnect oscilloscope and rms voltmeter. Set SD112-H RESPONSE switch to MED. Set RT for −20 dB attenuation (10000). Connect DVM to A2TP2.

b. Set RT for −40 dB (01000). Adjust A2R11 for 2V ±5 mV incremental change when switching RT from −20 dB to −40 dB.

NOTE

The absolute values of the voltages are not important. Some drift is normal, however, the incremental voltage should be 2V ±5 mV each time this point is checked.

Remove power, reinstall board A2 in its receptacle using the key.

4.5.7 Input Buffer/Log Converter A-C Operation (A1)

Set RT for −20 dB attenuation (10000). Connect DVM to A1TP10.

a. Adjust A1R38 for 2V ±5 mV incremental change when switching from −20 dB to −40 dB (01000).

NOTE

The absolute values of the voltages are not important. Some drift is normal, however, the incremental voltage should be 2V ±5 mV each time this point is checked.

b. At -40 dB input, adjust A1R36 for 5.985V ±5 mV.

c. Connect DVM to A1TP11, and adjust A1R56 for 5.985V ±5 mV.

d. Set RT for 0 dB (X0000), and adjust A3R17 (on board A3) for 10V ±25 mV. If necessary, select new factory adjustable resistor A3R16 to obtain 10V ±25 mV at A1TP11.

Set RT for -20 dB (10000) and connect DVM to A1TP13.

e. Adjust A1R50 for incremental change of 5 mV or less when switching RT from -20 dB to -40 dB.

Connect DVM to A1TP11.

f. With 0 dB attenuation inserted (X0000), ensure that SD104A supplies 1V ±10 mV rms measured at input of SD112-H. Set RT for 0 dB to -60 dB in 10 dB steps, and record voltages at A1TP11. Voltages should be as follows:

0 dB (X0000)	10V ±25 mV
-10 dB (31623)	9V ±25 mV
-20 dB (10000)	8V ±25 mV
-30 dB (03162)	7V ±25 mV
-40 dB (01000)	5.985V ±25 mV
-50 dB (00316)	5V ±25 mV
-60 dB (00100)	4V ±65 mV

Remove RT and connect SD104A directly to SD112-H INPUT. Adjust SD104A for approximately 10 mV rms at 400 Hz.

g. Use DVM Averager with DVM and measure approximately 5.985V at A1TP11.

h. Change SD104A frequency to 10 Hz. Check that DVM reading does not change more than ±45 mV from that measured in Step g.

i. Change SD104A frequency to 10 kHz. DVM reading should not change more than ±45 mV from that measured in Step g.

Remove DVM Averager (T70) and adjust SD104A for 1 Vrms at 400 Hz.

j. Set SD112-H INPUT RANGE switch to AC 10; DVM should indicate 8V ±55 mV.

k. Set SD112-H INPUT RANGE switch to AC 100; DVM should indicate 6V ±55 mV.

4.5.8 A-C Linearity Test

Set SD112-H INPUT RANGE switch to AC 1 and RESPONSE switch to MED. Reinsert the RT between SD104A and SD112-H; set to 0 dB attenuation (X0000). Adjust SD104A for 1V ±10 mV rms, 400 Hz at INPUT to SD112-H.

Connect CONSTANT AMPLITUDE OUTPUT (J19) of SD104A to TUNING INPUT of SD101B and select the 10 Hz filter (FILTER 2); connect DVM to A2TP2.

a. Switch RT from 0 to -10 dB attenuation (31623) and note incremental change of voltage at A2TP2.

b. Switch RT between -70 dB (00032) and -80 dB (00010) and note DVM change. Adjust A2R21 so change is same (±75 mV) as that noted in Step a.

c. With RT at -80 dB, note voltage at A2TP2; set SD112-H INPUT RANGE to AC 100, wait several seconds, and return to AC 1. A2TP2 voltage should return to value noted for AC 1 setting. Repeat this step again.

d. With RT at 0 dB (X0000), ensure that SD112-H INPUT is 1V ±10 mV. Set RT for 0 dB to −70 dB in 10 dB steps, and record the voltages at A1TP11 as follows:

0 dB (X0000)	10V ±25 mV
−10 dB (31623)	9V ±25 mV
−20 dB (10000)	8V ±25 mV
−30 dB (03162)	7V ±25 mV
−40 dB (01000)	5.985V ±25 mV
−50 dB (00316)	5V ±35 mV
−60 dB (00100)	4V ±45 mV
−70 dB (00032)	3V ±95 mV

4.5.9 Input Buffer/Log Converter D-C Operation (A1)

Set SD112-H INPUT RANGE (VOLTS) switch to DC 1. Connect DC ∝ FREQ OUTPUT (J23) on SD104A through HP350D (−20 dB) to SD112-H INPUT. Adjust SD104A for 100 mV ±0.2 mV measured at SD112-H INPUT. Connect DVM to A1TP11.

a. Adjust A1R62 for voltage (±3 mV) recorded in paragraph 4.5.7 f. (−20 dB setting). If necessary, select new factory adjustable resistor A1R14 to obtain proper reading.

b. Set HP350D to −50 dB, and adjust SD104A for 3.162 mV ±0.01 mV measured at SD112 INPUT. Adjust A1R5 for voltage (±3 mV) recorded in paragraph 4.5.7 f. (−50 dB setting).

NOTE

Some interaction exists between steps a. and b.; therefore, repeat them as necessary to achieve proper voltage measurements.

c. Apply 1V ±1 mV to SD112 INPUT, and adjust A3R11 (on board A3) for 10V ±25 mV at A1TP11. If necessary, select new factory adjustable resistor A3R10 to obtain proper reading.

d. Apply 100 mV ±0.1 mV to SD112-H INPUT. Change SD112-H INPUT RANGE switch from DC 1 to DC 10 and note voltage change at A1TP11 on DVM. Return switch to DC 1.

e. Apply 100 mV ±0.1 mV and then 10 mV ±0.01 mV to SD112-H INPUT, and note change indicated by DVM at A1TP11. DVM should change by same amount (±5 mV) as change noted in Step d. If not, adjust A1R8 so incremental change is same (±5 mV) for Steps d. and e.

f. Repeat step a.; then check step b.

g. Set SD112-H INPUT RANGE switch to DC 1, connect DVM to A1TP11, and note the voltages indicated for each input as follows:

INPUT	A1TP11
1.0000V	10V ±25 mV
0.3162V	9V ±25 mV
0.1000V	8V ±25 mV
0.316V	7V ±25 mV
0.0100V	5.985V ±25 mV
0.0032V	5V ±45 mV

4.5.10 Response Time (Without Filters)

On SD101B, set FILTER switch to OUT. Set SD112-H RESPONSE switch to slow.

Disconnect RT and connect HP350D Attenuator (0 dB) and T69, 40 dB switchable attenuator (0 dB) in series between SD104A and SD112-H. Adjust SD104A for 1V ±10 mV rms, 400 Hz at SD112-H INPUT. Then set HP350D for −10 dB attenuation.

Connect storage oscilloscope to A1TP11, and adjust it for d-c input, time base at 2 s/cm, and vertical sensitivity for 2V/cm.

NOTE

The response time is measured between the 10% and 90% points (not including overshoot time) observed on the oscilloscope memo trace. The T69, 40 dB switchable attenuator is used for all checks.

a. Switch in −40 dB attenuation; response time should be 6.5s ±2.6s.

b. Return switch to 0 dB; response time should be 6.5s ±2.6s.

Set SD112-H RESPONSE switch to MED.

c. Switch in −40 dB attenuation; response time should be 1.45s ±0.6s.

d. Return switch to 0 dB; response time should be 1.45s ±0.6s.

Set SD112-H RESPONSE switch to FAST.

e. Switch in 40 dB attenuation; response time should be 0.86s ±0.34s.

f. Return switch to 0 dB; response time should be 0.86s ±0.34s.

4.5.11 Stability Test (With Filters)

Set SD112-H RESPONSE switch to SLOW and INPUT RANGE switch to AC 1. On SD101B, set FILTER switch to 1 (2 Hz).

a. Connect oscilloscope to J9 and observe constant amplitude signal.

b. Switch SD112-H INPUT RANGE switch from AC 1 to AC 10 and back to AC 1 several times, and observe that constant amplitude signal does not oscillate.

In SD101B, remove 2 Hz filter (position 1) and insert a preheated 20 Hz filter. Set SD112-H RESPONSE switch to MED, and SD101B FILTER switch to FILTER 2 (10 Hz).

c. Repeat Step b.

Set SD112-H RESPONSE switch to FAST, and SD101B FILTER switch to 1 (20 Hz).

d. Repeat Step b.

4.5.12 Meter Circuit Adjustments

Disconnect HP350D and T69, 40 dB attenuator from test setup, and connect SD104A directly to SD112-H INPUT. Set SD112-H METER MULTIPLIER switch to 0 dB/1, and adjust SD104A for reading of 20 (−20 dB) on center scale of SD112-H VOLTS RMS/DC meter.

a. Connect DVM to A3TP1 and adjust A3R2 for 8V ±1 mV.

Connect DVM to A1TP11 and adjust SD104A for 10.01V $\binom{+10}{-0}$ mV.

b. Adjust A3R4 for 0 dB reading on center scale of SD112-H meter. If necessary, select new factory adjustable resistor A3R3 (or R13 on METER MULTIPLIER switch) to obtain 0 dB reading.

c. Set SD112-H METER MULTIPLIER switch to 0–80 dB/1, and adjust A3R5 for 0 dB reading on 0 to −80 dB meter scale.

4.5.13 Meter Calibration Check

Connect the RT between the SD104A and SD112-H. Set RT for 0 dB attenuation (X0000). On SD101, set FILTER switch to 1 (20 Hz). Set SD112-H RESPONSE switch to FAST, INPUT RANGE to AC 1, and METER MULTIPLIER to 0–80/1 (lower markings/upper markings). Monitor SD112-H INPUT with rms voltmeter and adjust SD104A for 1V ±10 mV rms.

Using the RT, vary the INPUT signal level in −10 dB increments from 0 to −80 dB. See Table 4-5 and check the VOLTS RMS/DC meter readings for each input value on both the 0–80/1 meter scale and the 0 to 20 dB expanded scale (in conjunction with appropriate setting of the METER MULTIPLIER switch). Note that the sequence of steps in Table 4-5 is designed to check calibration of the 0–80 dB scale, and both ends of the 0–20 dB expanded scale (for −20, −40 and −60 dB inputs) with minimum METER MULTIPLIER switching.

4.5.14 Y-CAL Calibration

On SD101B, set FILTER switch to OUT. Set ratio transformer for 0 dB attenuation (X0000). Ensure that SD104A supplies 1V ±10 mV rms to INPUT of SD112-H.

a. Connect DVM to LOG DC OUT connector J16; note reading (400 mV nominal).

b. Set SD112-H Y-CAL switch to CHAN 1, −10 dB; DVM reading should decrease by 100 mV ±0.1 mV. Adjust A1R72 for proper reading.

Return Y-CAL switch to OPER.

4.5.15 Squaring Circuit Accuracy Test

Monitor with rms voltmeter, and apply 1V ±10 mV rms, 400 Hz square wave directly to SD112-H INPUT.

a. Connect DVM to A1TP11 and read 10V ±40 mV.

Table 4-5. Volts rms/dc Meter Calibration Checks

Step	Input Level (dB)	Ratio Xfmr Setting	Meter Multiplier dB/Mult.	0–80 dB Scale Reading	0–20 dB Scale Reading
1	0	X0000	0–80/1	0 ±2	
2			0/1		0 ±0.35
3	–10	31623	0/1		–10 ±0.35
4			0–80/1	–10 ±2	
5	–20	10000	0–80/1	–20 ±2	
6			0/1		–20 ±0.35
7			–20/.1		0 ±0.35
8	–30	03162	–20/.1		–10 ±0.35
9			0–80/1	–30 ±2	
10	–40	01000	0–80/1	–40 ±2	
11			–20/.1		–20 ±0.35
12			–40/.01		0 ±0.35
13	–50	00316	–40/.01		–10 ±0.45
14			0–80/1	–50 ±2	
15	–60	00100	0–80/1	–60 ±2	
16			–40/.001		–20 ±0.55
17			–60/.001		0 ±0.55
18	–70	00032	–60/.001		–10 ±1
19			0–80/1	–70 ±2	
20	–80	00010	0–80/1	–80 ±2	
21			–60/.001		–20 ±2

b. Change input signal to triangular waveform at 1V ±10 mV rms and read 10V ±40 mV at A1TP11.

4.5.16 Crest Factor Check

Set SD112-H INPUT RANGE switch to AC 1 and METER MULTIPLIER to 0 dB/1. Connect HP202C to SD112-H INPUT and adjust for 400 Hz output.

Connect oscilloscope to A1TP3.

a. Increase 400 Hz signal level until clipping is observed on oscilloscope presentation; clipping should occur at 16V ±1V p-p.

NOTE

Paragraph 4.5.16 concludes the calibration of Channel 1. All SD112-H front panel controls, meter, and connectors referenced throughout the following paragraphs 4.5.17 through 4.5.29 are CHANNEL 2.

4.5.17 Input Buffer/Log Converter (A9)

Remove power, extend board A9, and reapply power.

a. Jumper A9TP2 to ground terminal on board A9 and connect DVM to A9TP3. Adjust A9R5 for 0V ±0.1 mV. Remove jumper at A9TP2.

Set INPUT RANGE (VOLTS) switch to DC 1, and connect DVM to A9TP6.

b. Jumper terminal at top end of A9R17 to either the -15V or +15V terminal above A9R17, which gives a DVM reading of 0V ±0.1 mV as adjusted by A9R18.

4.5.18 Amplifier/Detector Calibration (A8)

Remove power, replace board A9 in its receptacle (without nylon key), extend board A8, and reapply power. Remove left end of jumper wire above A8R16, -R12, -R19, -R17, and connect to GND terminal below A8R16. Remove one end of jumper wire at right side of A8R16.

a. Connect DVM to A8TP3, and adjust A8R21 for 0V ±0.1 mV.

b. Connect DVM to A8TP4. Jumper terminal at bottom end of A8R17 to either the -15V or +15V terminal, which gives a DVM reading of 0V ±0.1 mV as adjusted by A8R18.

c. Connect DVM to A8TP3; if necessary, readjust A8R21 for 0V ±0.1 mV.

Replace jumpers at right of A8R16 and above A8R16, -R12 etc. Remove coaxial jumper between CONSTANT AMPLITUDE OUTPUT/INPUT connectors J3 and J4 on chassis rear panel. On DVM, disconnect jumper between INPUT signal ground and chassis ground so DVM accepts differential input.

d. Connect DVM signal INPUT's to A8TP7 and A8TP8; adjust A8R51 for 0V ±10 mV.

NOTE

Because some noise exists at A8TP7 and A8TP8, adjust A8R51 for an average value.

4.5.19 Amplifier/Detector Operation (A8)

Install 2 Hz and 10 Hz filter units in positions 1 and 2 respectively in the SD101B. Ensure that all test equipment is warmed up and stabilized, and connect the SD112-H and test equipment as shown in Figure 4-8.

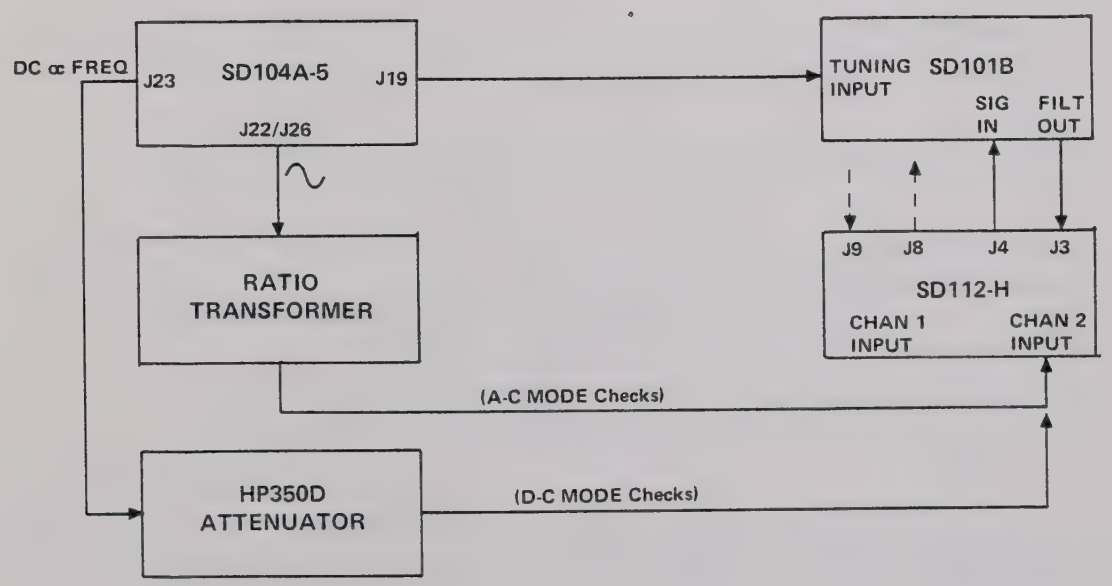


Figure 4-8. General Test Setup for Channel 2 Detailed Calibration

NOTE

Throughout the following procedures, the ratio transformer knob settings (left to right) are given in parenthesis after each attenuation value.

Set SD112-H INPUT RANGE (VOLTS) switch to AC 1. Set ratio transformer (RT) for 0 dB attenuation (X0000). Adjust the SD104A for sine wave output of 1 Vrms ±10 mV, 400 Hz, measured at SD112-H INPUT. Set SD101B RANGE switch to the .1 position and FILTER switch to OUT. Connect oscillsocope and rms voltmeter to Channel 1 CONSTANT AMPLITUDE INPUT J3.

a. Adjust A8R63 for 45 mV ±0.5 mV rms, clean sine wave at J3.

Disconnect oscilloscope and rms voltmeter. Set SD112-H RESPONSE switch to MED. Set RT for -20 dB attenuation (10000). Connect DVM to A8TP2.

b. Set RT for -40 dB (01000). Adjust A8R11 for 2V ±5 mV incremental change when switching RT from -20 dB to -40 dB.

Remove power, reinstall board A8 in its receptacle using nylon insert, extend board A9, and reapply power.

4.5.20 Input Buffer/Log Converter A-C Operation (A9)

Set RT for -20 dB attenuation (10000). Connect DVM to A9TP10.

a. Adjust RT for -40 dB (01000). Adjust A9R38 for 2V ±5 mV incremental change when switching from -20 dB to -40 dB (01000).

b. At -40 dB input, adjust A9R36 for 5.985V ±5 mV.

c. Connect DVM to A9TP11, and adjust A9R56 for 5.985V ±5 mV.

d. Set RT for 0 dB (X0000), and adjust A3R35 (on board A3) for 10V ±25 mV. If necessary, select new factory adjustable resistor A3R34 to obtain 10V ±25 mV at A9TP11.

Set RT for -20 dB (10000) and connect DVM to A9TP13.

e. Adjust A9R50 for incremental change of 5 mV or less when switching RT from -20 dB to -40 dB.

Remove power, connect an insulated test lead to A9TP11, and replace A9 in its receptacle (without extender board).

f. With 0 dB attenuation inserted (X0000), ensure that SD104A supplies 1V ±10 mV rms measured at input of SD112-H. Set RT for 0 dB to -60 dB in 10 dB steps, and record voltages at A9TP11. Voltages should be as follows:

0 dB (X0000)	10V ±25 mV
-10 dB (31623)	9V ±25 mV
-20 dB (10000)	8V ±25 mV
-30 dB (03162)	7V ±25 mV
-40 dB (01000)	5.985V ±25 mV
-50 dB (00316)	5V ±45 mV
-60 dB (00100)	4V ±65 mV

Remove RT and connect SD104A directly to SD112-H INPUT. Adjust SD104A for approximately 10 mV at 400 Hz.

g. Use DVM Averager with DVM and measure approximately 5.985V at A9TP11.

h. Change SD104A frequency to 10 Hz. Check that DVM reading does not change more than ±45 mV from that measured in step g.

i. Change SD104A frequency to 10 kHz. DVM reading should not change more than ±45 mV from that measured in step g.

j. Remove T70 DVM Averager, apply 1 Vrms, 400 Hz to INPUT, and set SD112-H INPUT RANGE switch to AC 10; DVM should indicate 8V ±55 mV.

k. Set SD112-H INPUT RANGE switch to AC 100; DVM should indicate 6V ±55 mV.

4.5.21 A-C LinearityTest

Set SD112-H INPUT RANGE switch to AC 1 and RESPONSE switch to MED. Reinsert the RT between SD104A and SD112-H; set to 0 dB attenuation (X0000). Adjust SD104A for 1V ±10 mV rms, 400 Hz, at INPUT to SD112-H.

Connect CONSTANT AMPLITUDE OUTPUT (J19) of SD104A to TUNING INPUT of SD101B and select the 10 Hz filter (FILTER 2); connect DVM to A2TP2.

a. Switch RT from 0 to −10 dB attenuation (31623) and note incremental change of voltage at A8TP2.

b. Switch RT between −70 dB (00032) and −80 dB (00010) and note DVM change. Adjust A8R21 so change is same (±75 mV) as that noted in Step a.

c. With RT at −80 dB, note voltage at A8TP2; set SD112-H INPUT RANGE to AC 100, wait several seconds, and return to AC 1. A8TP2 voltage should return to value noted for AC 1 setting. Repeat this step again.

d. With RT at 0 dB (X0000), ensure that SD112-H INPUT is 1V ±10 mV. Set RT for 0 dB to −70 dB in 10 dB steps and record the voltages at A9TP11 as follows:

0 dB (X0000)	10V ±25 mV
−10 dB (31623)	9V ±25 mV
−20 dB (10000)	8V ±25 mV
−30 dB (03162)	7V ±25 mV
−40 dB (01000)	5.985V ±25 mV
−50 dB (00316)	5V ±35 mV
−60 dB (00100)	4V ±45 mV
−70 dB (00032)	3V ±95 mV

4.5.22 Input Buffer/Log Converter D-C Operation (A9)

Set SD112-H INPUT RANGE (VOLTS) switch to DC 1. Connect DC ∝ FREQ OUTPUT (J23) on SD104A through HP350D (−20 dB) to SD112-H INPUT. Adjust SD104A for 100 mV ±0.2 mV measured at SD112-H INPUT. Connect DVM to A9TP11.

a. Adjust A9R62 for voltage (±3 mV) recorded in paragraph 4.5.20 f. (-20 dB setting). If necessary, select new factory adjustable resistor A9R14 to obtain proper reading.

b. Set HP350D to -50 dB, and adjust SD104A for 3.162 mV ±0.001 mV measured at SD112-H INPUT. Adjust A9R5 for voltage (±3 mV) recorded in Paragraph 4.5.20 f. (-50 dB setting).

NOTE

Some interaction exists between steps a. and b.; therefore, repeat them as necessary to achieve proper voltage measurements.

c. Apply 1V ±1 mV to SD112-H INPUT, and adjust A3R29 (on board A3) for 10V ±25 mV at A9TP11. If necessary, select new factory adjustable resistor A3R28 to obtain proper reading.

d. Apply 100 mV ±0.1 mV to SD112-H INPUT. Change SD112-H INPUT RANGE switch from DC 1 to DC 10 and note voltage change at A9TP11 on DVM. Return switch to DC 1.

e. Apply 100 mV ±0.1 mV and then 10 mV ±0.01 mV to SD112-H INPUT, and note change indicated by DVM at A9TP11. DVM should change by same amount (±5 mV) as change noted in Step d. If not, adjust A9R8 so incremental change is same (±5 mV) for Steps d. and e.

f. Repeat Step a,; then check Step b.

g. Set SD112-H INPUT RANGE switch to DC 1, connect DVM to A9TP11, and record the voltages indicated for each input as follows:

Input	A9TP11
1.0000V	10V ±25 mV
0.3162V	9V ±25 mV
0.1000V	8V ±25 mV
0.0316V	7V ±25 mV
0.0100V	59.85V ±25 mV
0.0032V	5V ±45 mV

4.5.23 Response Time (Without Filters)

On SD101B, set FILTER switch to OUT. Set SD112-H RESPONSE switch to SLOW. Disconnect RT and connect HP350D Attenuator (0 dB) and T69, 40 dB switchable attenuator (0 dB) in series between SD104A and SD112-H. Adjust SD104A for 1V ±10 mV rms, 400 Hz at SD112-H INPUT. Then set HP350D for – 10 dB attenuation.

Connect storage oscilloscope to A9TP11, and adjust it for d-c input, time base at 2 s/cm, and vertical sensitivity for 2V/cm.

NOTE

The response time is measured between the 10% and 90% points (not including overshoot time) observed on the oscilloscope memo trace. The T69, 40 dB switchable attenuator is used for all checks.

a. Switch in –40 dB attenuation; response time should be 6.5s ±2.6s.

b. Return switch to 0 dB; response time should be 6.5s ±2.6s.

On SD112, set RESPONSE switch to MED.

c. Switch in –40 dB attenuation; response time should be 1.45s ±0.6s.

d. Return switch to 0 dB; response time should be 1.45s ±0.6s.

On SD112, set RESPONSE switch to FAST.

e. Switch in –40 dB attenuation; response time should be 0.86s ±0.34s.

f. Return switch to 0 dB; response time should be 0.86s ±0.34s.

4.5.24 Stability Test (With Filters)

On SD112-H set RESPONSE switch to SLOW and INPUT RANGE switch To AC 1.

On SD101B, set FILTER switch to 1 (2 Hz).

a. Connect oscilloscope to J3 and observe constant amplitude signal.

b. Switch SD112-H INPUT RANGE switch from AC 1 to AC 10 and back to AC 1 several times, and observe that constant amplitude signal does not oscillate.

In SD101B, remove 2 Hz filter (position 1) and insert a preheated 20 Hz filter. Set SD112-H RESPONSE switch to MED, and SD101B FILTER switch to FILTER 2 (10 Hz).

c. Repeat step b.

Set SD112-H RESPONSE switch to FAST, and SD101B FILTER switch to 1 (20 Hz).

d. Repeat step b.

4.5.25 Meter Circuit Adjustments

Disconnect HP350D and T69, 40 dB attenuator from test setup, and connect SD104A directly to SD112-H INPUT. Set SD112-H METER MULTIPLIER switch to 0 dB/1, and adjust SD104A for reading of 20 (-20 dB) on center scale of SD112-H VOLTS RMS/DC meter.

a. Connect DVM to A3TP2 and adjust A3R20 for 8V ±1 mV.

Connect DVM to A9TP11 and adjust SD104A for 10.01V $\binom{+10}{-0}$ mV.

b. Adjust A3R22 for 0 dB reading on center scale of SD112-H meter. If necessary, select new factory adjustable resistor A3R21 (or A3R31 on METER MULTIPLIER switch) to obtain 0 dB reading.

c. Set SD112-H METER MULTIPLIER switch to 0–80 dB/1, and adjust A3R23 for 0 dB reading on 0 to -80 dB meter scale.

4.5.26 Meter Calibration Check

Connect the RT between the SD104A and SD112-H. Set RT for 0 dB attenuation (X0000). On SD101B, set FILTER switch to 1 (20 Hz). Set SD112-H RESPONSE switch to FAST, INPUT RANGE to AC 1 and METER MULTIPLIER to 0–80/1 (lower markings/upper markings). Monitor SD112-H INPUT with rms voltmeter and adjust SD104A for 1V ±10 Mv rms.

Using the RT, vary the INPUT signal level in -10 dB increments from 0 to -80 dB. See Table 4-5 and check the VOLTS RMS/DC meter readings for each input value on both the 0—80/1 meter scale and the 0 to 20 dB expanded scale (in conjunction with appropriate setting of the METER MULTIPLIER switch).

4.5.27 Y-CAL Calibration

On SD101B, set FILTER switch to OUT. Set ratio transformer to 0 dB attenuation (X0000). Ensure that SD104A supplies 1V ±10 mV rms to INPUT of SD112-H.

a. Connect DVM to LOG DC OUT connector J17; note reading (400 mV nominal).

b. Set SD112 Y-CAL switch to CHAN 2, -10 dB; DVM reading should decrease by 100 mV ± 0.1 mV. Adjust A9R72 for proper reading.

Return Y-CAL switch to OPER.

4.5.28 Squaring Circuit Accuracy Test

Monitor with rms voltmeter, and apply 1V ±10 mV rms, 400 Hz square wave directly to SD112-H INPUT.

a. Connect DVM to A9TP11 and read 10V ± 40 mV.

b. Change input signal to triangular waveform and read 10V ±40 mV at A9TP11.

4.5.29 Crest Factor Check

Set SD112-H INPUT RANGE switch to AC 1 and METER MULTIPLIER to 0 dB/1. Connect HP202C to SD112-H and adjust for 400 Hz output. Connect oscilloscope to A9TP3.

a. Increase 400 Hz signal level until clipping is observed on oscilloscope presentation; clipping should occur at 16V ±1V p-p.

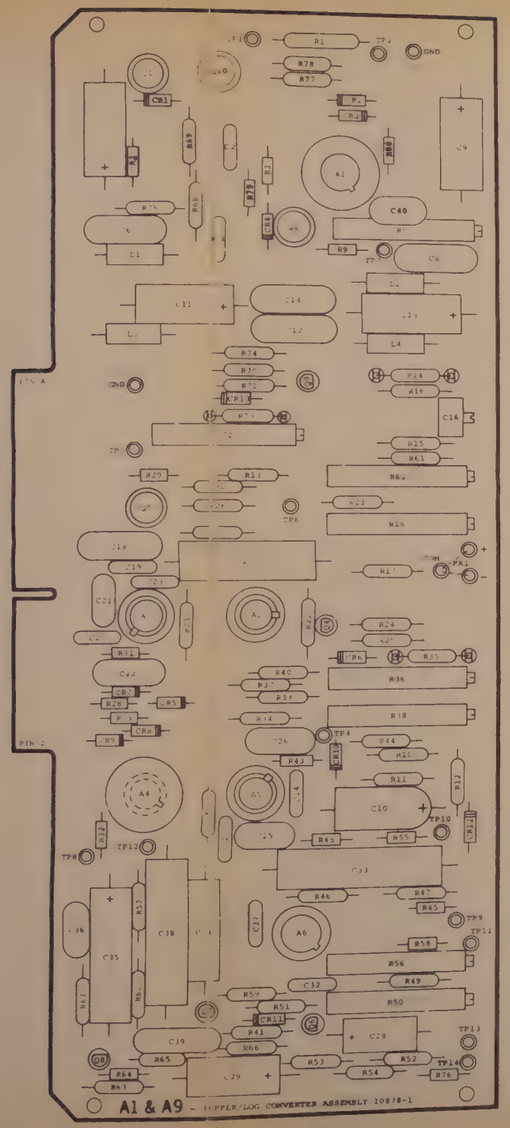
4.5.30 Channel 1 Meter Circuit Final Adjustment

Disconnect the HP202C and connect SD104A directly to SD112-H CHANNEL 1 INPUT. Set SD112-H CHANNEL 1 METER MULTIPLIER switch to 0 dB/1. Connect DVM to A1TP11, and adjust SD104A for $10.01V\binom{+10}{-0}$ mV on DVM.

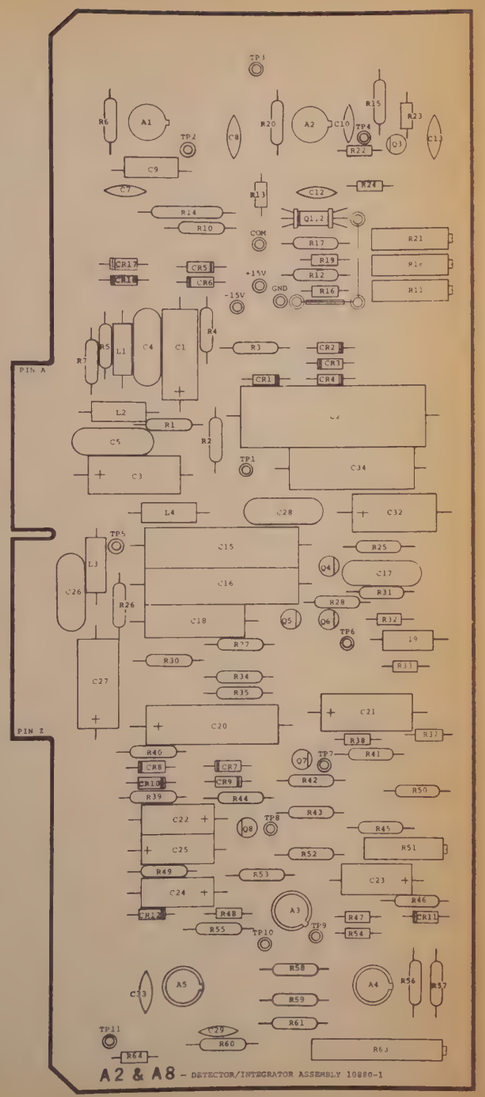
a. Adjust A3R4 for 0 dB reading on center scale of SD112 CHANNEL 1 meter.

b. Set SD112-H CHANNEL 1 METER MULTIPLIER switch to 0—80 dB/1, and adjust A3R5 for 0 dB reading on 0 to −80 dB meter scale.

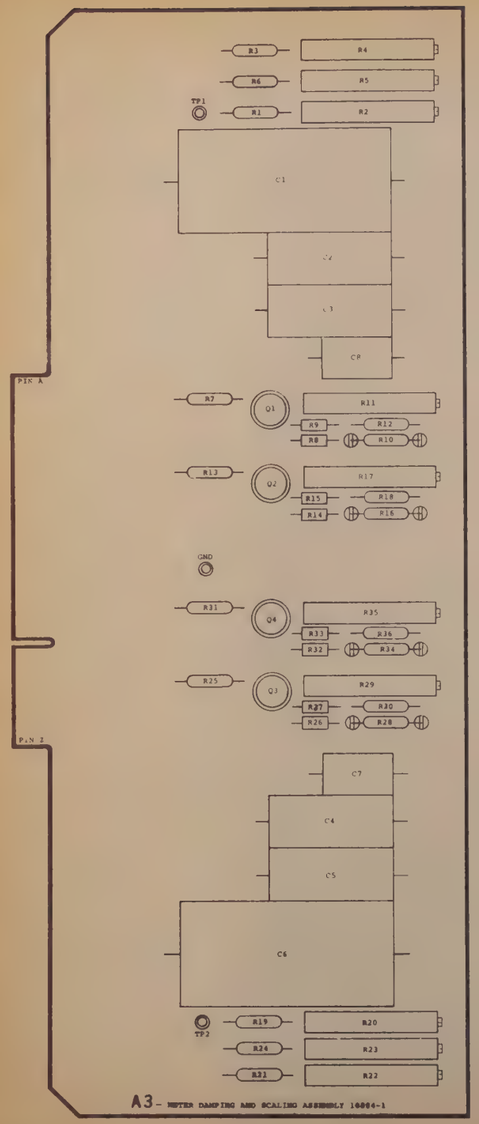
This concludes the detailed calibration procedure. Remove power and disconnect all test equipment. Replace the top chassis cover plate and return the instrument to service.



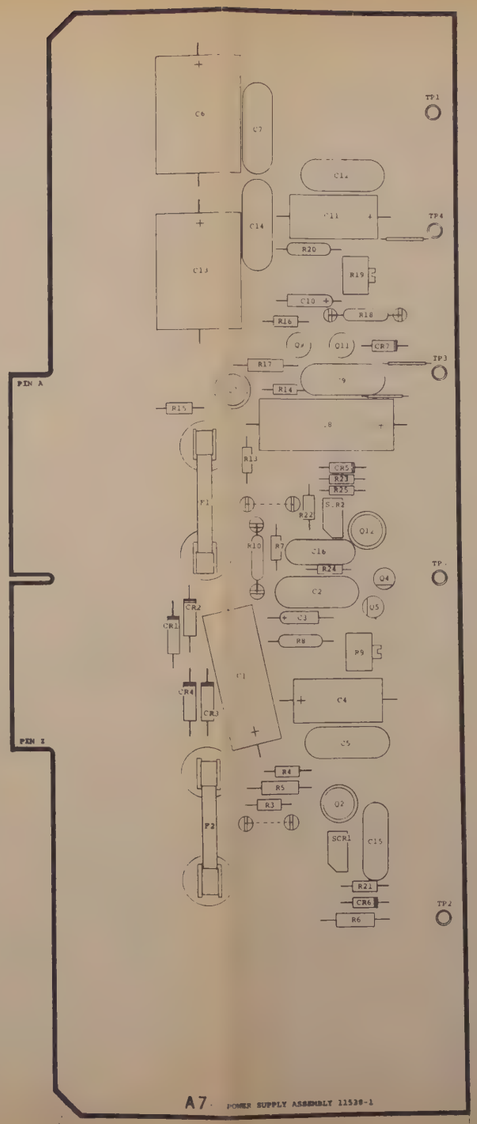
A1 & A9 - BUFFER/LOG CONVERTER ASSEMBLY 10878-1



A2 & A8 - DETECTOR/INTEGRATOR ASSEMBLY 10880-1



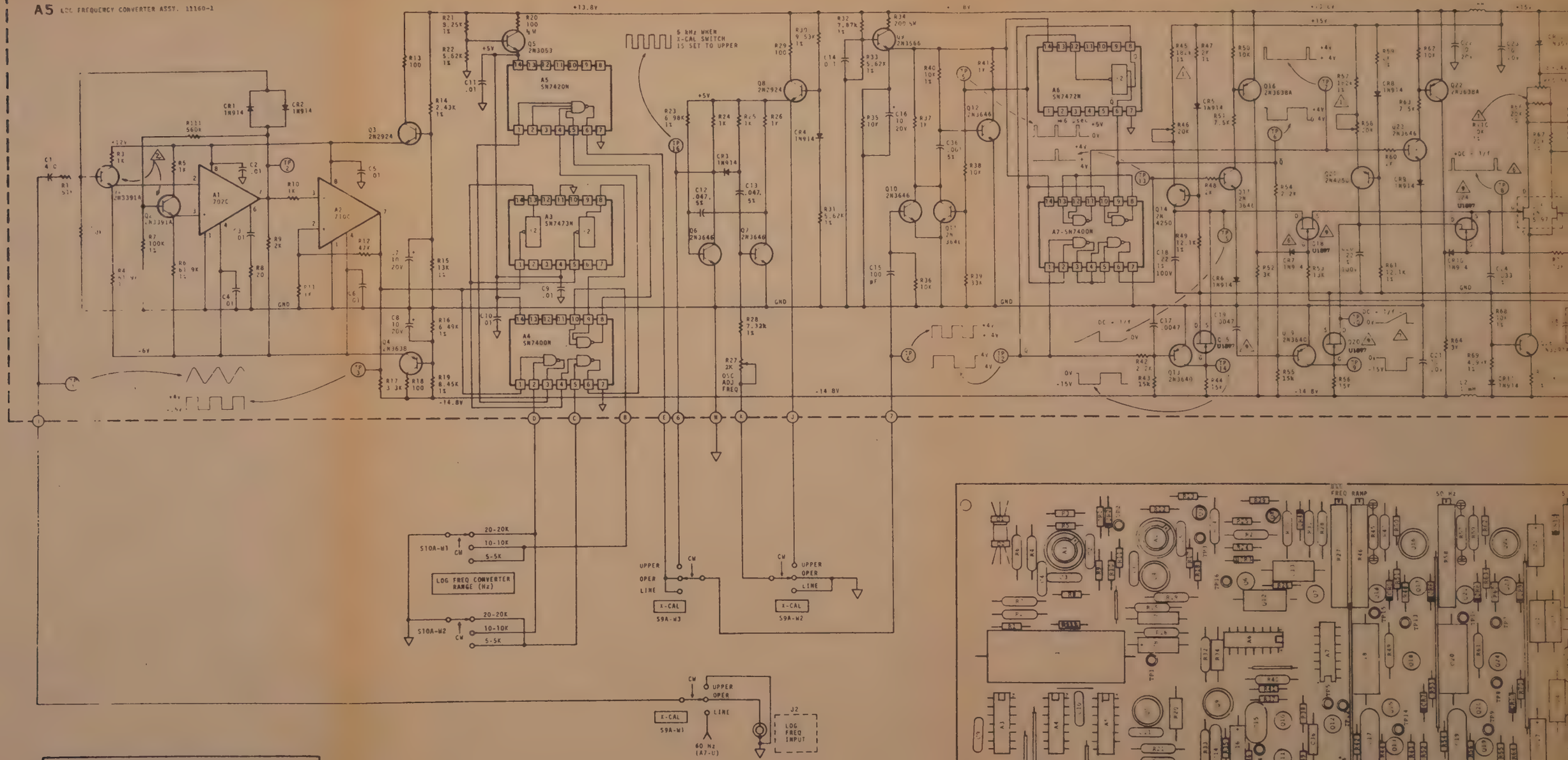
A3 - METER DAMPING AND SCALING ASSEMBLY 10884-1

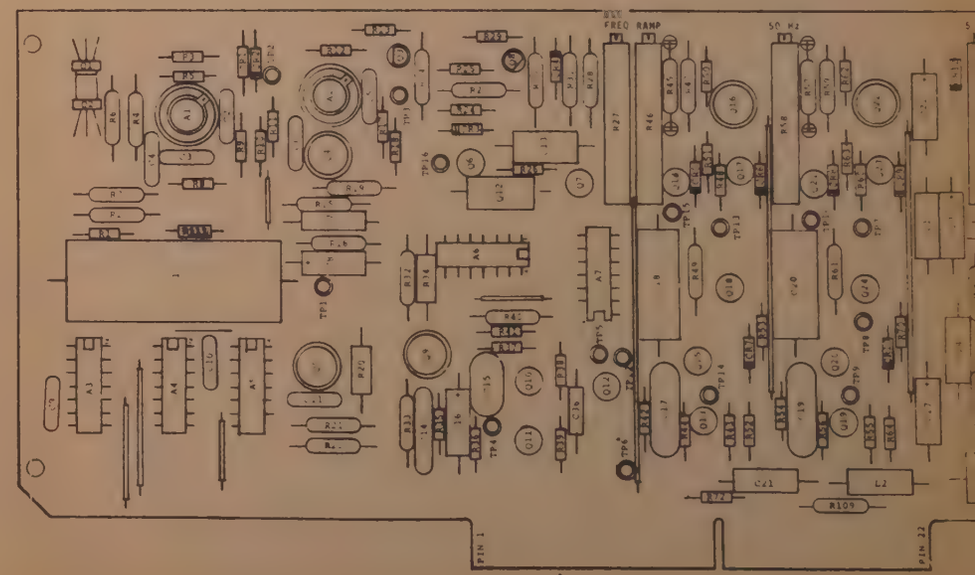


A7 - POWER SUPPLY ASSEMBLY 11538-1

SPECTRAL DYNAMICS CORPORATION OF SAN DIEGO		TITLE: COMPONENT LAYOUT - Model SD112-H Voltmeter/Log Converter	
DRAWN	A. L. Clark	SIZE:	DRAWING NO: 10928
CHECKED	[illegible]		REV: X
ENGINEER	[illegible]	SCALE	SHEET 2 OF 2
APPROVED	[illegible]		

A5 LOG FREQUENCY CONVERTER ASSY. 11160-1





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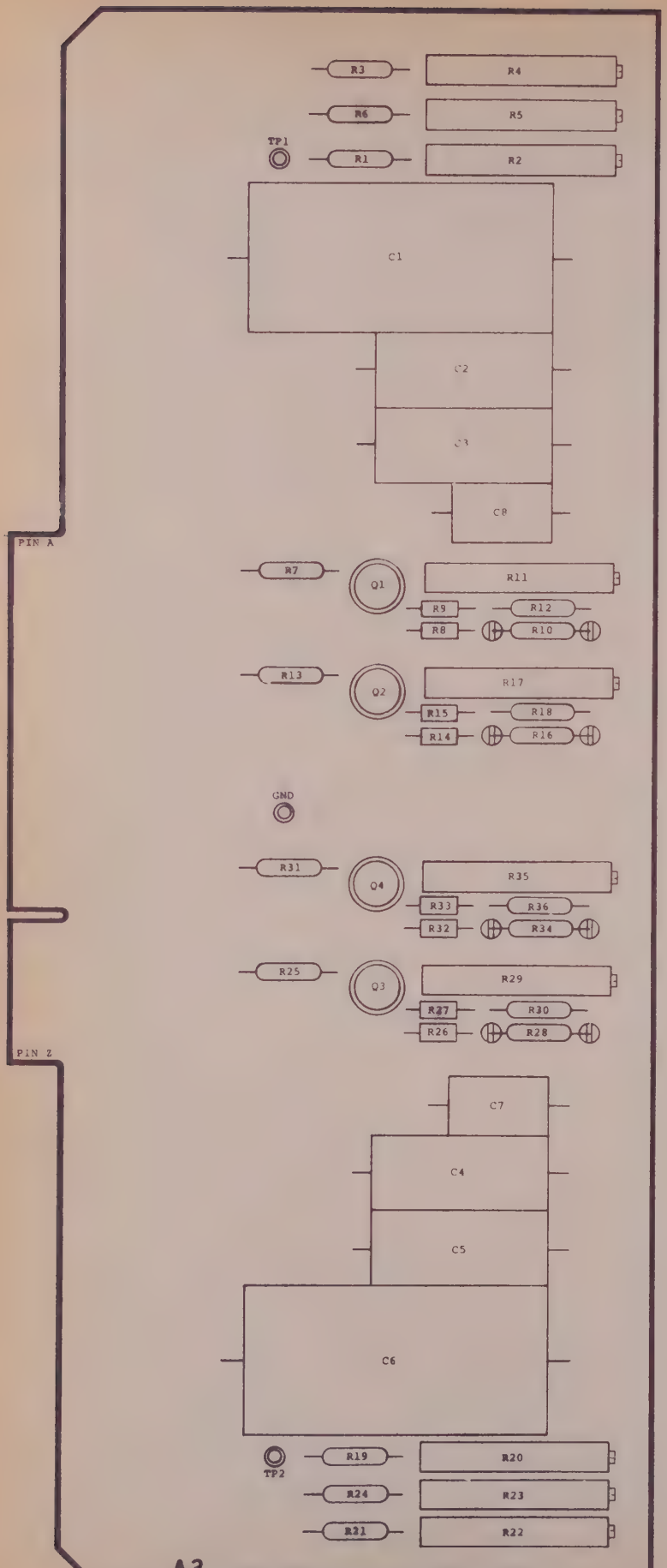
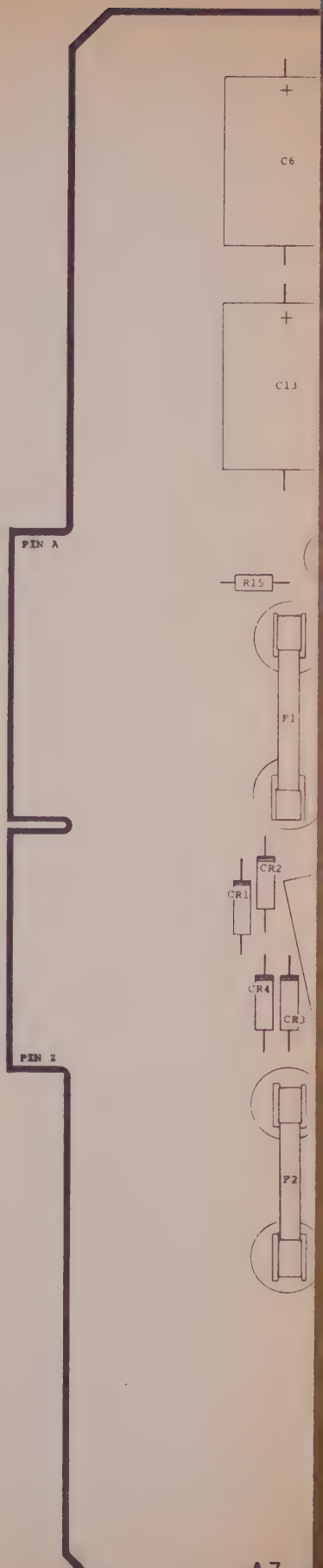


A3 - METER DAMPING AND SCALING ASSEMBLY 10004-1



A7

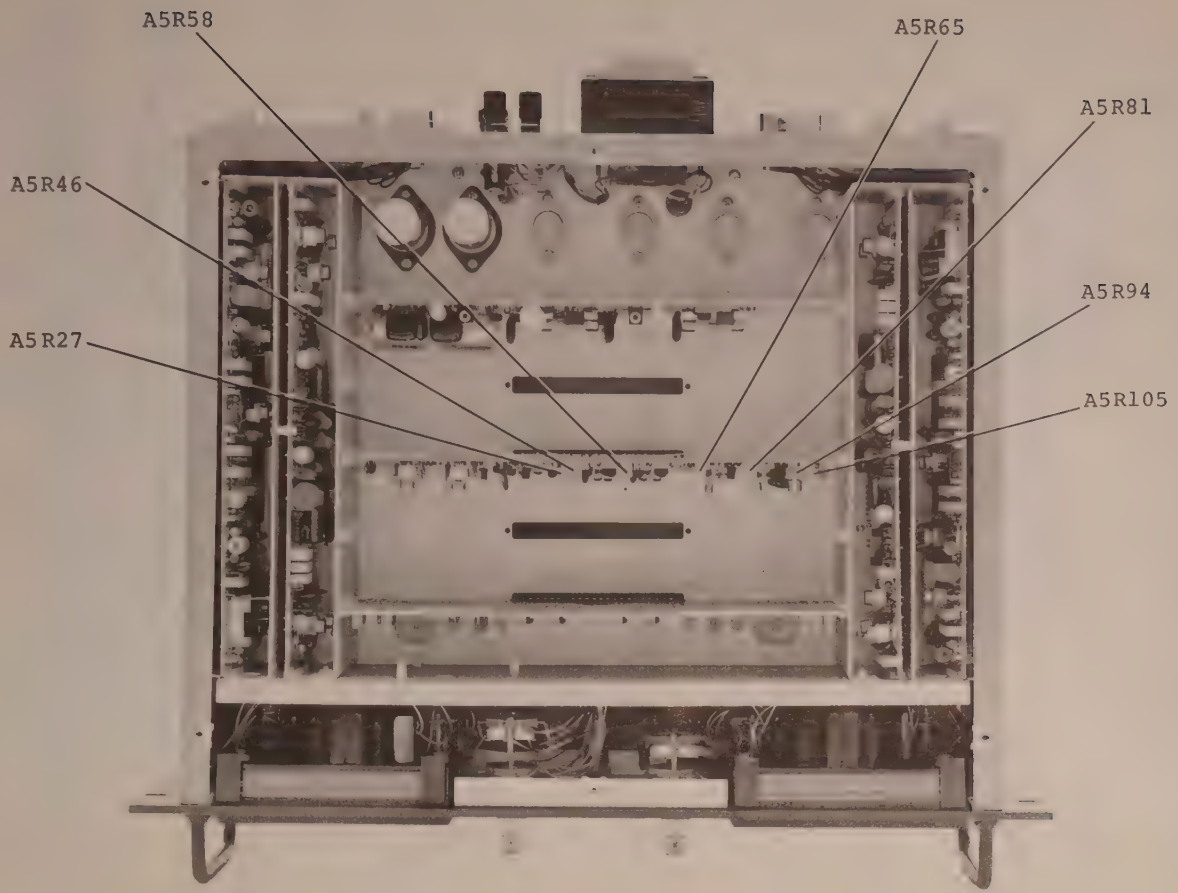


Figure 4-1. Top Chassis View – Calibration Controls (SD112-1-H Only)

SERIAL _____

Instruction Manual Addendum

SD112-1-H

VOLTMETER/FREQUENCY LOG CONVERTER

(MODIFIED TO MODEL SD112-1-H-3)

U.S. PATENT NO. 3,502,959; PATENT PENDING

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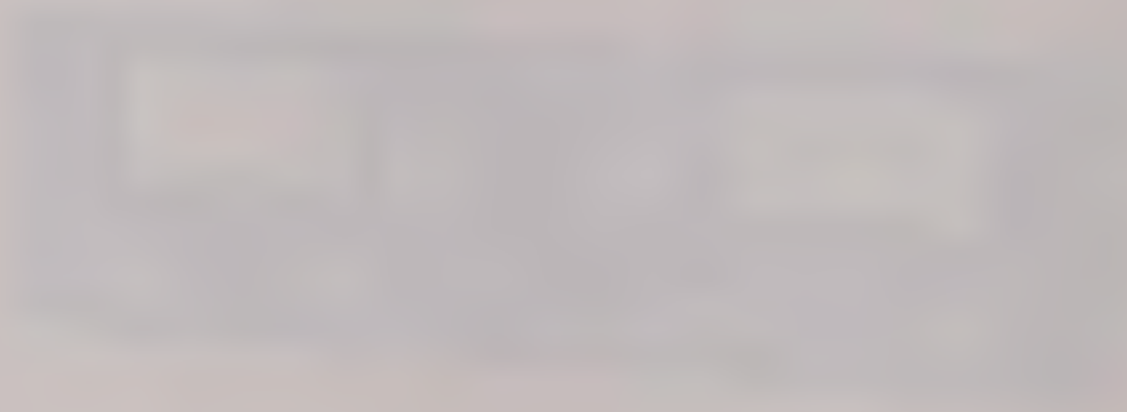
December 1977

MODEL SD112-1-H VOLTMETER/FREQUENCY LOG CONVERTER



HARDWARE
WARRANTY POLICY

All products manufactured by Spectral Dynamics are warranted against defects in materials and workmanship for one year from the date of delivery or, in the case of certain components listed in some of the operating manuals, for the specified period. We will repair or replace products which prove defective during the warranty period, providing the failure or damage has not been caused by misuse or abnormal operating conditions.

If the malfunction or a portion thereof is determined by Spectral Dynamics Corporation to have been caused by misuse or abnormal conditions of operation, an estimate of cost to repair will be submitted to the purchaser for approval before beginning any repair work.

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If a malfunction develops, notify the Customer Service Department of Spectral Dynamics Corporation or its representative in your area, giving details of the problem and the name, model and serial number of the equipment. Upon receipt of this information, service data or shipping instructions will be provided.

Spectral Dynamics Corporation
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S-072
August 1977

PREFACE

RECEIVING INSPECTION PROCEDURE

The Model SD112-1-H Voltmeter/Frequency Log Converter is shipped in a manner designed to protect it against normal shipping hazards. Immediately upon receipt, inspect and note any apparent visible damage. Keep all forms and invoices. Test its operation and if shipping damage is apparent, file a claim with the carrier's claims agent and send a copy to Spectral Dynamics Corporation. Be sure to include the system name, model number, and serial number on all correspondence. Spectral Dynamics Corporation will advise the buyer what should be done; arrangements for repair or replacement will be made as applicable.

RETURN SHIPMENT PROCEDURE

On receipt of shipping instructions, forward the instrument prepaid via air freight to the factory or authorized repair station indicated on the instructions. Replace the instrument in its original shipping case or equivalent container.

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DWG. NO. 11136 Schematic/Component Layout, Log Frequency Converter Circuit Card A5 . . Rear

SECTION I

GENERAL INFORMATION

1.1 INTRODUCTION

This addendum describes the log frequency converter circuitry of the Model SD112-1-H Voltmeter/ Frequency Log Converter. The Model SD112-1-H is basically a Model SD112-H with an additional circuit that provides a d-c output proportional to the log of the input frequency. Therefore, the user is advised to study carefully Sections I, II, and III of the SD112-H Instruction Manual for the overall operation of this instrument.

1.2 BASIC OPERATION

The log frequency converter will accept any shape periodic waveform, sine wave to pulse with 10% or greater duty cycle, over the frequency range of 5 Hz to 20 kHz (in three decade intervals) and produce a d-c output of 0 to 1.000 volt proportional to the log of the frequency.

The a-c input is applied to the limiter circuit (see Figure 1-1) which provides a constant amplitude square-wave signal to the frequency divider flip-flops. In the 5-Hz to 5-kHz range, the limiter output is gated through to the voltage ramp generators. In the 10-Hz to 10-kHz and 20-Hz to 20-kHz ranges, the limiter output is divided by 2 and 4 respectively; thus the input to the voltage ramp generators is always 5 Hz to 5 kHz.

Two out-of-phase voltage ramps are generated and are then alternately sampled for peak amplitude. The stored sample, a d-c voltage inversely proportional to the input frequency, is applied to an FET (field-effect transistor) amplifier. In turn, the FET produces a d-c control current (inversely proportional to frequency) which controls the log converter. Thus the log converter d-c output is proportional to the log of the input frequency. The d-c output varies from 0 to 1.000 volt proportional to the log of the input frequency for each operating range.

An internal 2-kHz oscillator and the line frequency are used to provide recorder (plotter) calibration points at an upper and a lower reference point.

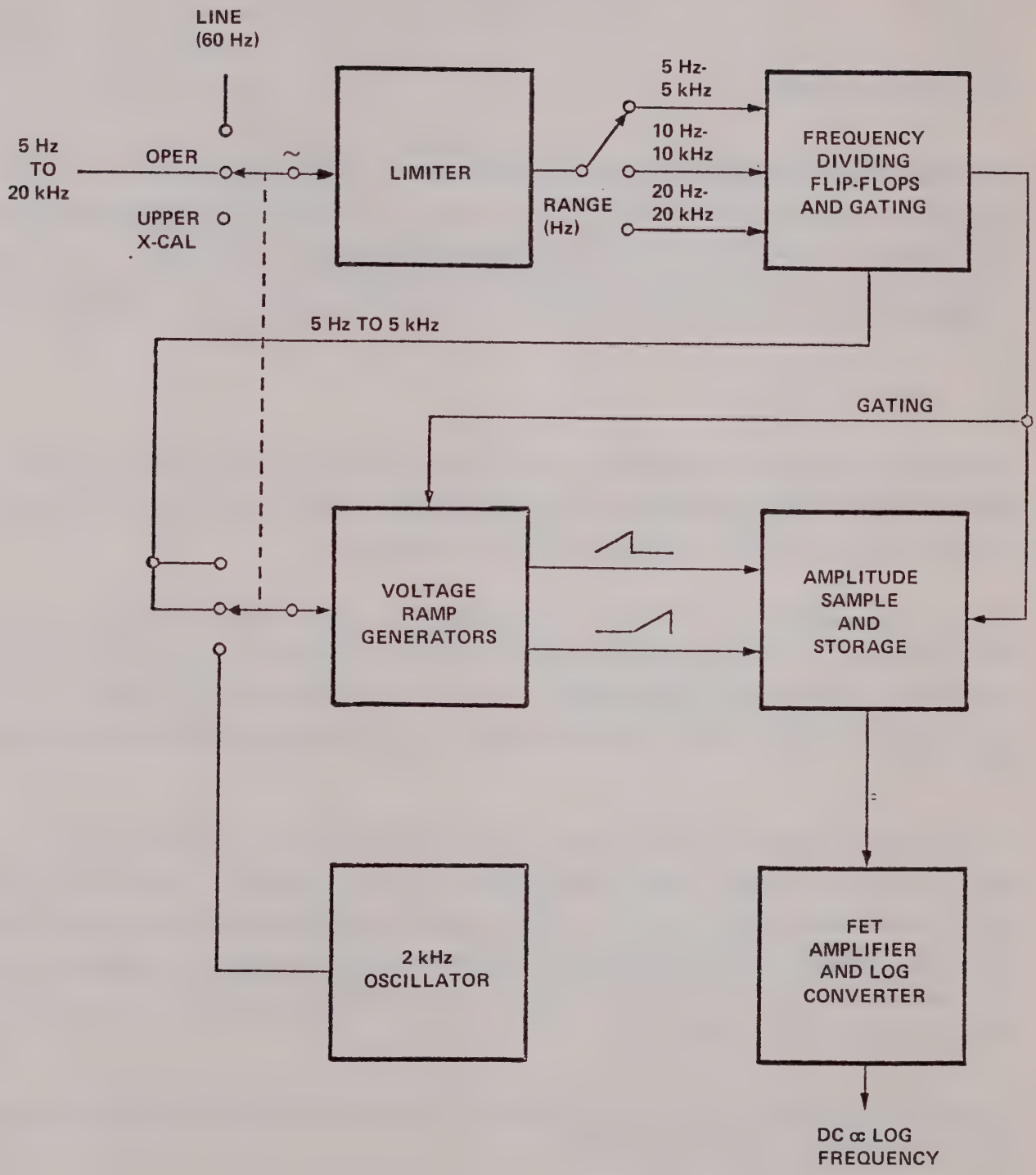


Figure 1-1. Simplified Block Diagram of Log Frequency Converter

1.3 FRONT PANEL FUNCTIONAL DESCRIPTION

Figure 1-2 illustrates the instrument front panel followed by a brief description of the front panel functions pertinent to a Model SD112-1-H.

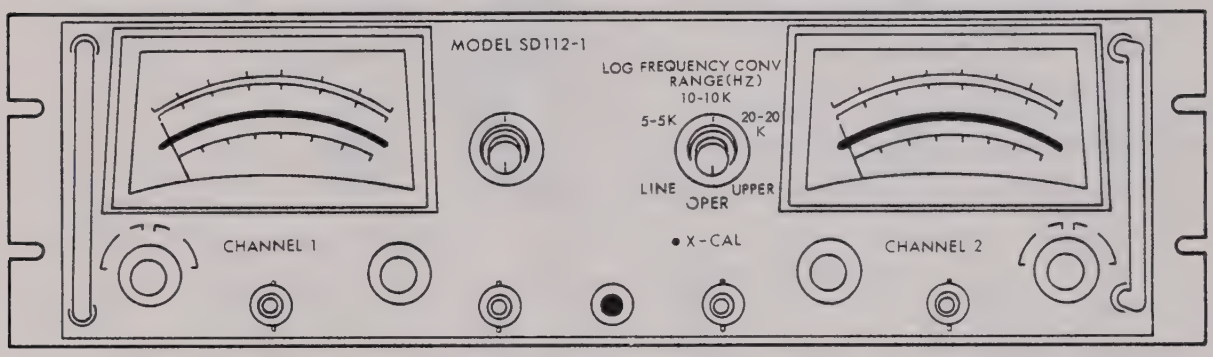


Figure 1-2. Front Panel

LOG FREQUENCY CONV RANGE (Hz)

This dual control switch performs the following two functions:

RANGE (Hz)

Outside (larger) knob selects frequency range (5 Hz—5 kHz, 10 Hz—10 kHz, 20 Hz—20 kHz) of log frequency converter.

X-CAL

Inside (smaller) knob facilitates recorder X-axis calibration: selects LINE (60 Hz) for lower calibration point, or UPPER (internal oscillator) for upper frequency reference point (2/5 full scale range selected).

1.4 REAR OF CHASSIS FUNCTIONAL DESCRIPTION

Figure 1-3 illustrates the rear of the instrument chassis followed by a brief description of the input/output functions pertinent to a Model SD112-1-H.

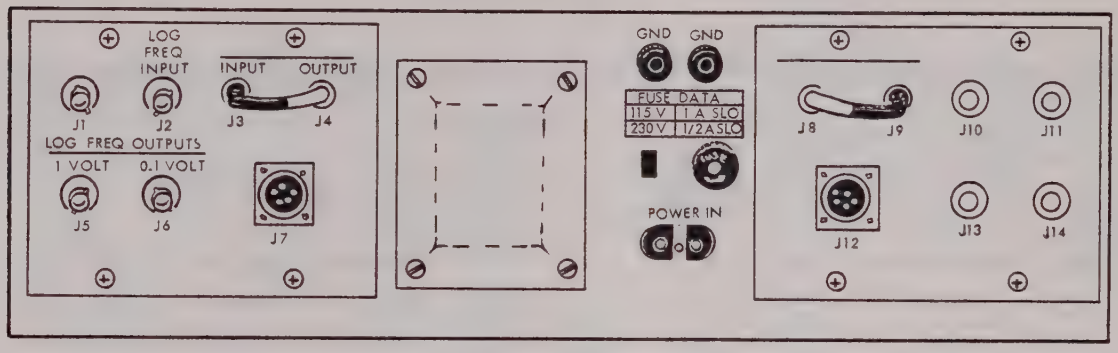


Figure 1-3. Rear of Chassis

LOG FREQ OUTPUTS

Used for connecting the dc ∝ log frequency output to recording or other peripheral test equipment. 1 VOLT and 0.1 VOLT outputs provide d-c voltages, 0 to 1 volt and 0 to 0.1 volt respectively, proportional to the logarithm of the input frequency over the selected range.

LOG FREQ INPUT

Accepts input frequency signal source; i.e., any shape periodic waveform, sine wave to pulse with 10% or greater duty cycle, over the frequency range of 5 Hz to 20 kHz.

1.5 SPECIFICATIONS

INPUT

Frequency . . . . . 5 Hz to 20 kHz

Ranges . . . . . 5 Hz to 5 kHz, 10 Hz to 10 kHz, 20 Hz to 20 kHz

*→ Waveform . . . . . Any shape periodic, sine wave to pulse with 30% or greater duty cycle

Impedance . . . . . >40 kilohms

Voltage Amplitude . . . . . Any level from 0.2V p-p to 100V p-p

OUTPUT

Voltage (nominal) . . . . . Two simultaneously available log d-c outputs with nominal sensitivities of 333-1/3 mV and 33-1/3 mV per decade (no linear d-c output):

5000 Hz ≈ 100 mV 500 Hz ≈ 66-2/3 mV 50 Hz ≈ 33-1/3 mV 5 Hz ≈ 0	for 5-Hz to 5-kHz range, proportional in upper two ranges

Ripple . . . . . Less than 1% of full-scale output voltage level

Impedance . . . . . 50 ohms nominal at 0.1V output (short-circuit proof)

500 ohms nominal at 1V output (short-circuit proof)

NORMALIZED CONVERSION ACCURACY (Conformance to Log Curve) . . . . . ±2% of frequency ±0.002% of full-scale frequency range

RESPONSE TIME . . . . . Inversely proportional to frequency: ≈500 ms at 5 Hz, and ≈25 ms at 20 kHz

CALIBRATION . . . . . Calibration of recorder facilitated by two front panel selected frequencies: line frequency (60 Hz) for lower reference point, and internal oscillator provides upper frequency reference point, 2/5 full scale of range selected.

*(Revised 6-21-73)

SECTION II

OPERATION

2.1 INTRODUCTION

This section provides instructions for using the log frequency converter in the Model SD112-1-H. Refer to the Model SD112-H Instruction Manual for all other operating procedures.

2.2 CONTROLS, INDICATORS AND CONNECTORS

All controls, indicators and connectors are identified and their operations are described on Figures 1-2 and 1-3 in Section I of this addendum.

2.3 OPERATING INSTRUCTIONS

a. Connect the frequency signal source to LOG FREQ INPUT connector J2 on the instrument rear panel.

b. Select either LOG FREQ OUTPUTS connector, 1 VOLT (J5) or 0.1 VOLT (J6) as applicable to the recorder input requirements.

c. On the front panel, set the LOG FREQUENCY CONV RANGE (Hz) to the desired frequency range. Ensure that the X-CAL switch is set to OPER.

d. Refer to Section II of the SD112-H Instruction Manual and perform the turn-on procedure. Make any other connections and preliminary control settings as applicable to the overall usage of the instrument in the particular installation.

2.4 RECORDER X-AXIS CALIBRATION

When the Model SD112-1-H is used in a mechanical impedance (MZ) measuring system, the dc $\propto$ log frequency is normally connected to the Model SD127 MZ/TFA Control for use in MZ computations and to the recorder X-axis input. The recorder X-axis can be calibrated as follows:

a. On the SD112-1-H front panel, set the X-CAL switch to LINE. Adjust recorder controls to place X-axis pen over the 60-Hz lower reference point.

b. Set the X-CAL switch to UPPER, and adjust the recorder GAIN control to place the X-axis pen over the upper frequency reference point (2 kHz, 4 kHz or 8 kHz).

c. Repeat steps a. and b. as required to compensate for any interaction.

d. After calibration is complete, return the X-CAL switch to OPER.

SECTION III

THEORY OF OPERATION

3.1 INTRODUCTION

This section describes the theory of operation of the log frequency converter circuitry in the Model SD112-1-H Voltmeter/Frequency Log Converter.

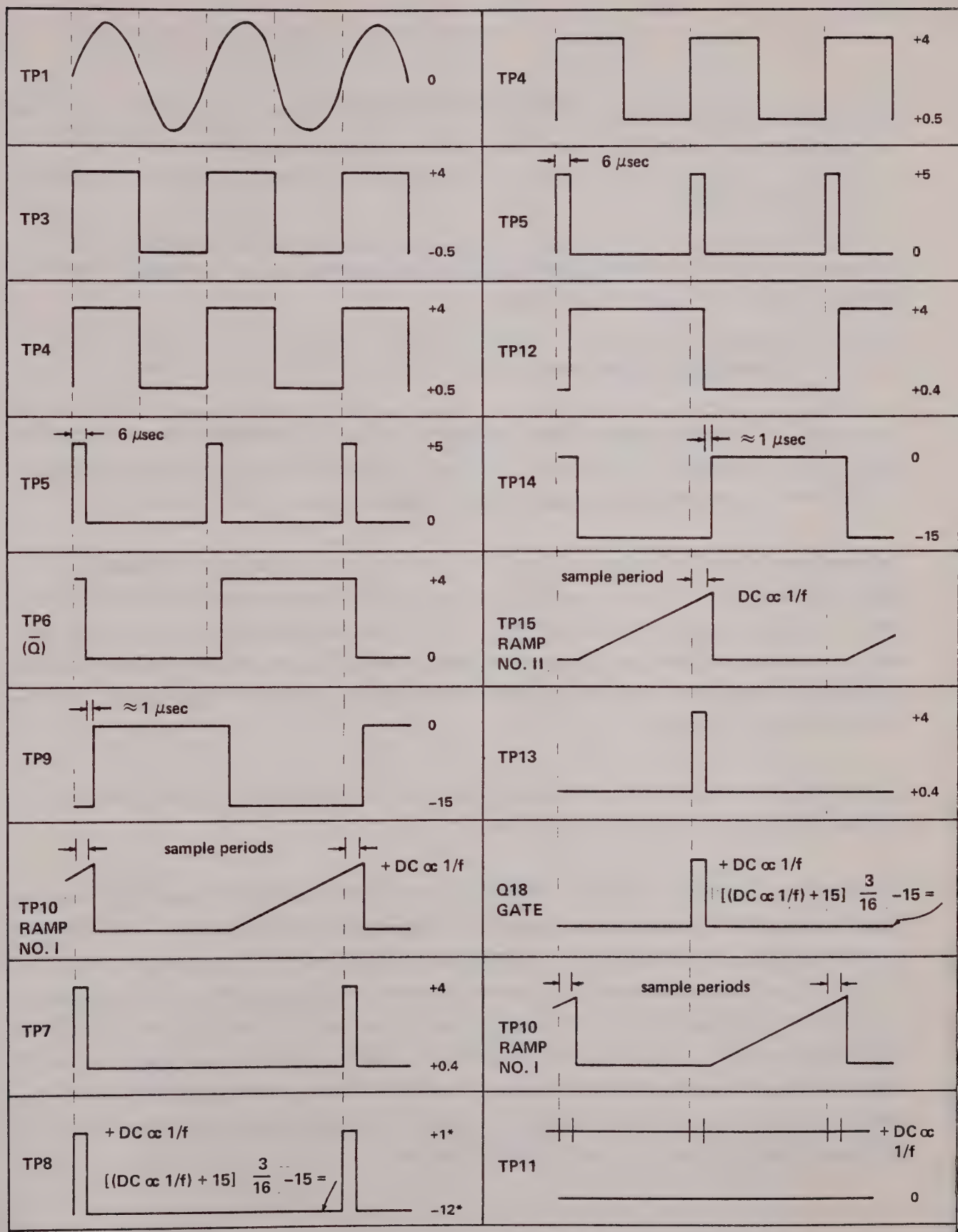
3.2 BLOCK DIAGRAM DISCUSSION

Throughout the following discussion, refer to Figures 3-1 and 3-2. Figure 3-2 is a functional block diagram of the log frequency converter circuit. The input and output of each main subcircuit is identified by a test point; the associated waveforms are shown in Figure 3-1.

The waveforms in the first column of Figure 3-1, from top to bottom, depict the development of the input sine wave at TP1 to ramp No. I at TP10, followed by its associated sample/transfer pulses (TP7 and TP8). For ease of comparison in timing, TP4 and TP5 have been repeated at the top of the second column. The waveforms in this column depict the development of ramp No. II, followed by its associated sample/transfer pulses (TP13 and Q18-G). Then TP10 is repeated to show the combination of TP10 and TP15 to form TP11 (+DC$\propto$1/f).

For this discussion, assume an input signal of 1 kHz, 0.5V p-p, sine wave. The X-CAL switch is set to OPER and the RANGE (Hz) switch is set to 5-5K.

The 1-kHz signal applied at LOG FREQ INPUT (J2) is routed through X-CAL switch S9A to the input limiter. Here the 1-kHz sine wave is converted to a constant-amplitude ($\approx$4.5V p-p) 1-kHz square-wave signal for application to the frequency dividing flip-flops. With the RANGE (Hz) switch set to 5-5K (Hz), the 1-kHz signal is routed through to the one-shot; therefore, the signal at TP4 is a 1-kHz square-wave signal, $\approx$4.5V p-p. Note that if the RANGE (Hz) switch was set to 10-10K (Hz) or 20-20K (Hz), a frequency division of 2 or 4 would be done to produce a 500-Hz or 250-Hz signal respectively at TP4. The log frequency converter circuitry between TP4 and TP18 always operates over the frequency range 5 Hz to 5 kHz; therefore frequency division is performed on all signals above 5 kHz; the divisor (2 or 4) being determined by the setting of the RANGE (Hz) switch.



*Voltages from formulas, f at TP4 = 50 Hz.

Figure 3-1. Logic Timing Diagram

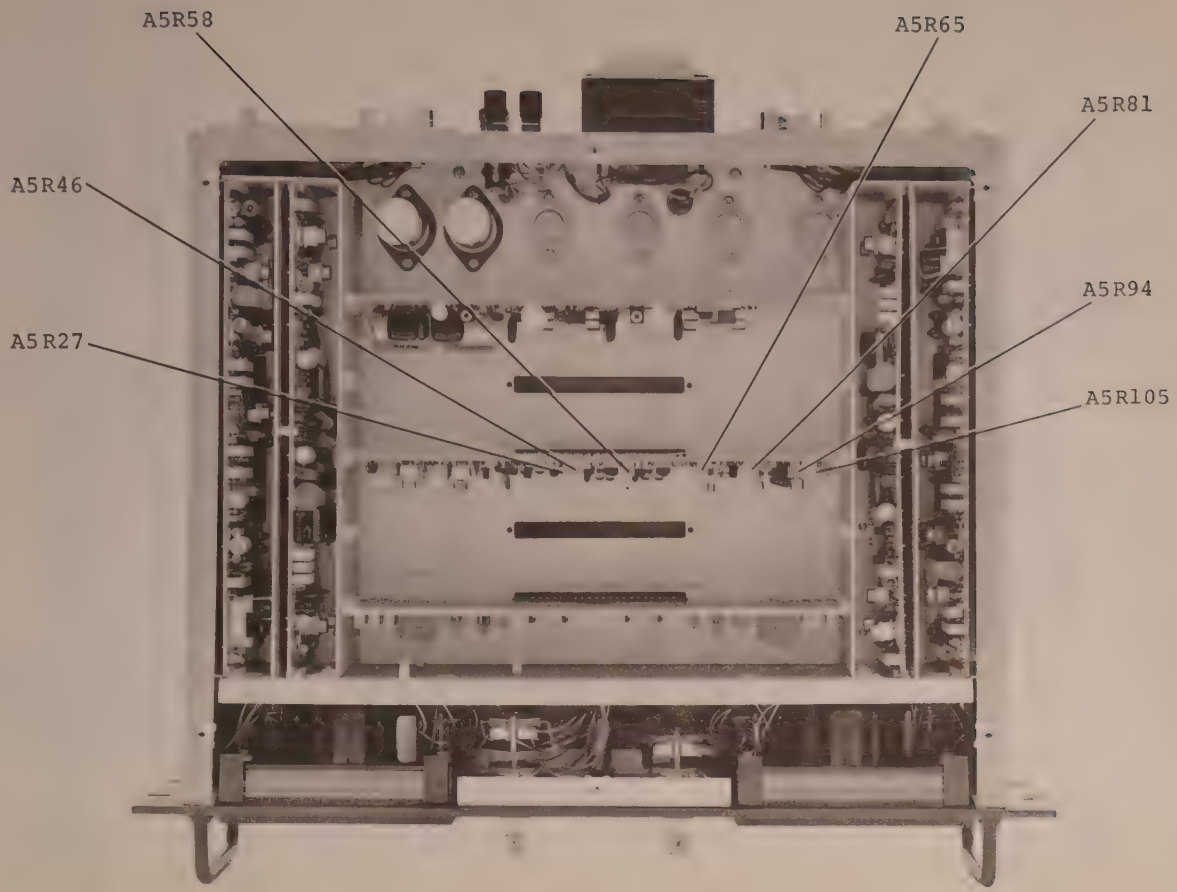


Figure 4-1. Top Chassis View — Calibration Controls (SD112-1-H Only)

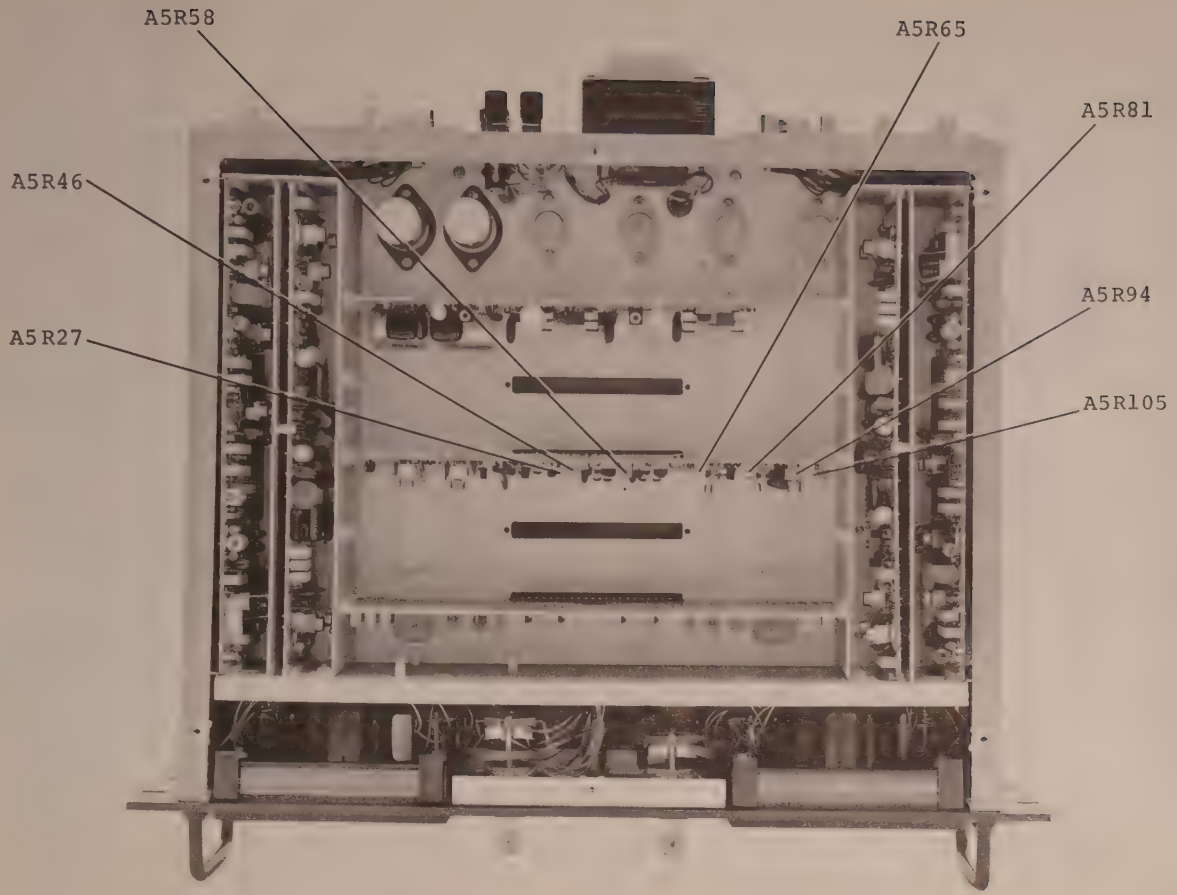


Figure 4-1. Top Chassis View — Calibration Controls (SD112-1-H Only)

See Figure 3-2 and note the placement of the X-CAL switch in the overall circuit. This switch facilitates recorder calibration at the line frequency (60 Hz) and an upper frequency reference point of any range selected. With S9A set to UPPER, the 2-kHz oscillator signal applied to the one-shot at TP4 produces a LOG FREQ OUTPUT of 0.867 Vdc. With S9A set to LINE, the 60-Hz ac is routed through, divided by two, or divided by four as determined by the RANGE (Hz) switch setting, and produces a dc $\propto$ log frequency 60 Hz, the amplitude being relative to the particular range. In like manner, all input frequencies are processed to produce a dc $\propto$ log input frequency, the amplitude being relative to 1 Vdc as determined by the particular RANGE (Hz) switch setting.

The one-shot produces 6-μs pulses at TP5 which drive the $\div 2$ flip-flop. The two flip-flop outputs, $\overline{Q}$ and Q, along with the 6-μs pulses (TP5) are used to develop alternately the two voltage ramps and transfer their peak amplitude (dc $\propto$ 1/f) into hold capacitor C24.

$\overline{Q}$ (TP6) is inverted and scaled to form TP9 which is used to develop ramp No. I. $\overline{Q}$ and TP5 are AND'ed (in series NAND gates of element A7) to form TP7. TP7 is scaled to produce TP8 which samples the peak amplitude of ramp No. I (TP10) and transfers it to hold capacitor C24.

Q(TP12) is inverted and scaled to form TP14 which is used to develop ramp No. II. Q and TP5 are AND'ed in element A7 to form TP13. TP13 is scaled to produce voltage at Q18-gate which samples the peak amplitude of ramp No. II (TP15) and transfers it to hold capacitor C24.

Compare the timing relationships of TP1, TP4, TP15, and TP10, and note that hold capacitor C24 is pulsed once each cycle to maintain its charge equal to dc $\propto$ 1/f. The component values have been chosen to accommodate rapid frequency changes at either end of the input spectrum, never requiring more than two input frequency cycles (at TP4) to charge C24 to dc $\propto$ 1/f.

The voltage charge in C24 is sensed by a high-impedance input FET (field effect transistor) operational amplifier circuit, and then buffered by a voltage follower for application to the log converter.

The voltage at TP11 (dc $\propto$ 1/f) controls the current flow into the log converter. The log converter is basically an operational amplifier with its gain controlled by the feedback current through a transdiode. Because of the nonlinear characteristics of the transdiode, the current flowing through it develops a new voltage that is proportional to the logarithm of the input voltage. (Its output is also inverted.) Therefore, the output of the log converter at TP17 is a d-c voltage proportional to the log of the input frequency.

The dc $\propto$ log frequency is buffered and routed to LOG FREQ OUTPUT connector J5. A precision 10:1 attenuator provides a 0 to 0.1V output at J6.

3.3 THEORY OF OPERATION

The following subparagraphs describe in detail the circuits of the log frequency converter. Because digital logic circuitry is used, a brief description of the logic elements and their operation is given in paragraph 3.3.1. Throughout the circuit descriptions, refer to Figures 3-1 and 3-2, and to the schematic diagram located at the back of this addendum.

NOTE

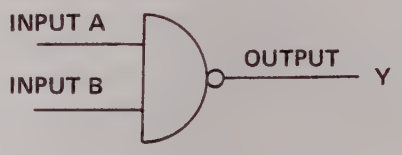
Because all parts referenced throughout the following circuit descriptions are located on circuit card A5 (except switches S9A and S10A), for the sake of clarity the prefix "A5" has been deleted from all parts designators.

3.3.1 Digital Logic Elements

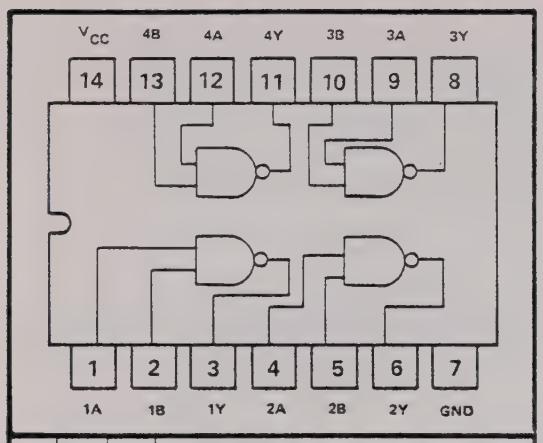
Four standard types of Texas Instrument Series 74 digital logic elements are used as follows: SN7473N Dual J-K Master-Slave Flip-Flop, SN7400N Quadruple 2-Input Positive NAND Gate, SN7420N Dual 4-Input Positive NAND Gate, and SN7472N J-K Master-Slave Flip-Flop. Figure 3-3 shows the logic symbol and element internal wiring connections for each type, along with their associated truth table.

Positive logic is used throughout the NAND gating circuitry: i.e., a logic "1" or "enable" is +2.4V to +5.5V (4V nominal) or an open circuit; a logic "0" or "disable" is 0V to 0.4V or ground.

The operation of a typical NAND gate is as follows:

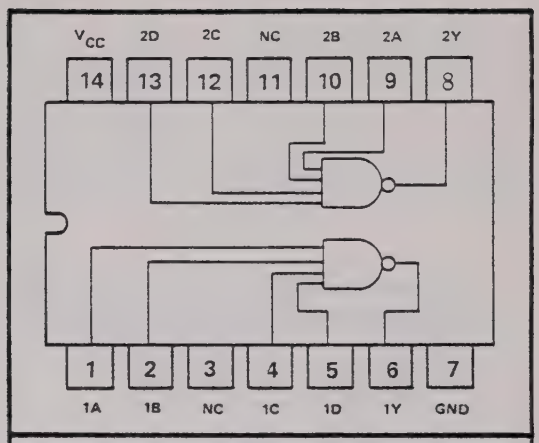


Using positive logic, both inputs A and B must be a logic "1" to produce a logic "0" at output Y. All other combinations of inputs produce a "1" at Y.

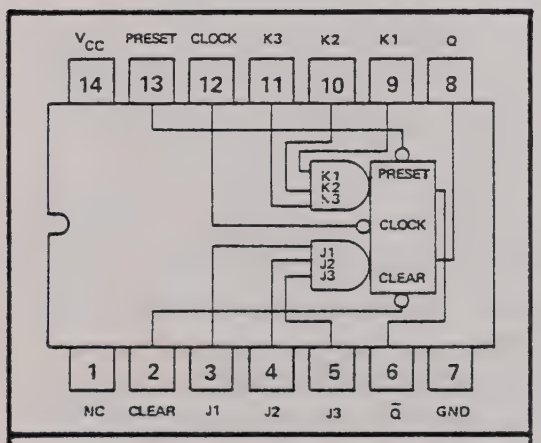


1A	1B	1Y
1	1	0
1	0	1
0	1	1
0	0	1

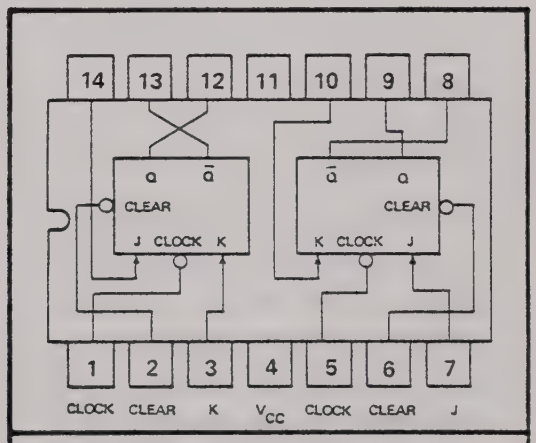
SN7400N
QUADRUPLE 2-INPUT
POSITIVE NAND GATE



SN7420N
DUAL 4-INPUT
POSITIVE NAND GATE



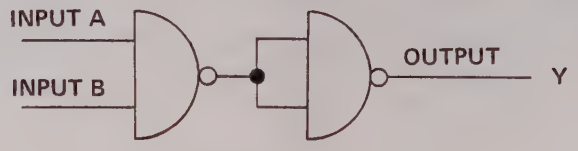
SN7472N
J–K MASTER–SLAVE
FLIP-FLOP



SN7473N
DUAL J–K MASTER–SLAVE
FLIP-FLOP

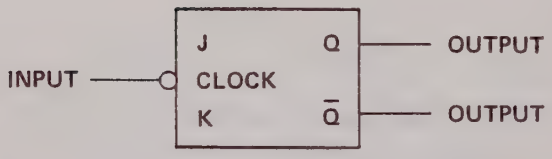
Figure 3-3. Digital Logic Elements

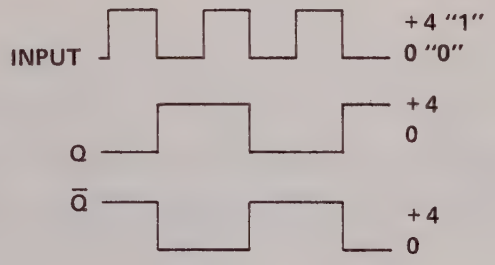
When two NAND gates are connected in series as shown below, the total circuit performs the AND function as follows:



Because the second NAND gate inverts its inputs, using positive logic, both inputs A and B must be a logic "1" to produce a logic "1" at output Y. All other combinations of inputs produce a "0" at Y.

Three J-K flip-flop circuits are used; each operates as follows: As shown in the waveform timing diagram for the J-K flip-flop, the outputs Q and $\overline{Q}$ change logic state only on the negative-going CLOCK input; i.e., when the CLOCK input changes from a "1" to a "0".





3.3.2 Input Limiter

The input limiter circuit will accept any shape periodic waveform, sine wave to pulse with 10% or greater duty cycle, over the frequency range of 5 Hz to 20 kHz, with an amplitude from 0.1V to 100V p-p. Its output (TP3) is a constant amplitude square-wave signal, ≈4.5V p-p, whose frequency is in phase with and equal to the input (TP1).

Transistors Q1 and Q2, element A1, and diodes CR1 and CR2 are connected as an operational amplifier. This amplifier operates linearly over the input voltage range; feedback via CR1 and CR2 prevents input overloading. The output of element A1 is a square wave signal, nominally 1V p-p, that drives element A2.

Element A2 operates as a differential comparator with (+) input pin 2 referenced to ground. When (−) input pin 3 is 1 mV or more below ground, the output (TP3) is ≈+4V; when pin 3 is 1 mV or more above ground, the output is ≈−0.5V.

3.3.3 Range Switching (Frequency Division)

The log frequency converter circuitry, between TP4 (at input to Q10) and TP18 (dc $\propto$ log frequency), operates over the frequency range of 5 Hz to 5 kHz. Therefore, INPUT frequencies in the 10-Hz to 10-kHz range are divided by two, and frequencies in the 20-Hz to 20-kHz range are divided by four. This frequency division is accomplished by dual flip-flop element A3 in conjunction with three 2-input NAND gates in element A4, one 4-input NAND gate in element A5, and RANGE (Hz) switch S10A. (See Figure 3-4.)

In the 5-Hz to 5-kHz range, S10A grounds (applies logic "0") A4-5 and A4-10. In this condition, A4-8 and A4-6 are logic "1"s, enabling A5-5 and A5-4 respectively. Because A4-2 is enabled (open or logic "1"), the INPUT passes through and is inverted by A4-2 and A4-3. Because A5-5 and A5-4 are enabled ("1"), A5-2 accepts the output of A4-3 and inverts it, and thus the output at A5-6 is the same frequency as the INPUT.

In the 10-Hz to 10-kHz range, S10A-W1 grounds A4-10, making A4-8 a "1" enabling A5-5. S10A-W2 grounds (disables) A4-2 making A4-3 a "1" to enable A5-1 and -2. Note that with A4-2 disabled, the INPUT at A4-1 has no affect. A4-5 is enabled (open or logic "1"); therefore f/2 from A3-13 can pass through A4-4 to A4-6, and subsequently through A5-4 to A5-6. The output frequency at A5-6 is now one-half the input frequency.

In the 20-Hz to 20-kHz range, S10A disables A4-5 and A4-2; A4-10 is open (enabled). In this condition, A4-6 and A4-3 are "1"s enabling A5-4 and A5-2, –1. A4-8 (A5-5) changes state inversely as A4-9. Therefore, only f/4 from A3-8 can pass through A4-9 to A4-8, and subsequently through A5-5 to A5-6. The output at A5-6 is now one-fourth the INPUT frequency.

3.3.4 X-CAL

The X-CAL switch (S9A) facilitates recorder calibration at two frequencies: LINE frequency (60 Hz) and an upper frequency reference, 2/5 full scale range selected.

With X-CAL switch S9A set to LINE, approximately 75 volts, 60-Hz ac from the power supply is applied through S9A-W1 to the limiter input (TP1). Therefore, a d-c voltage proportional to 60 Hz is provided at the output (TP18). The amplitude is relative to the RANGE (Hz) switch setting; i.e., the dc $\propto$ log 60 Hz is 3.6V, 2.6V, and 1.6V ($\pm$24 mV) for RANGE (Hz) settings 5-5K, 10-10K and 20-20K respectively.

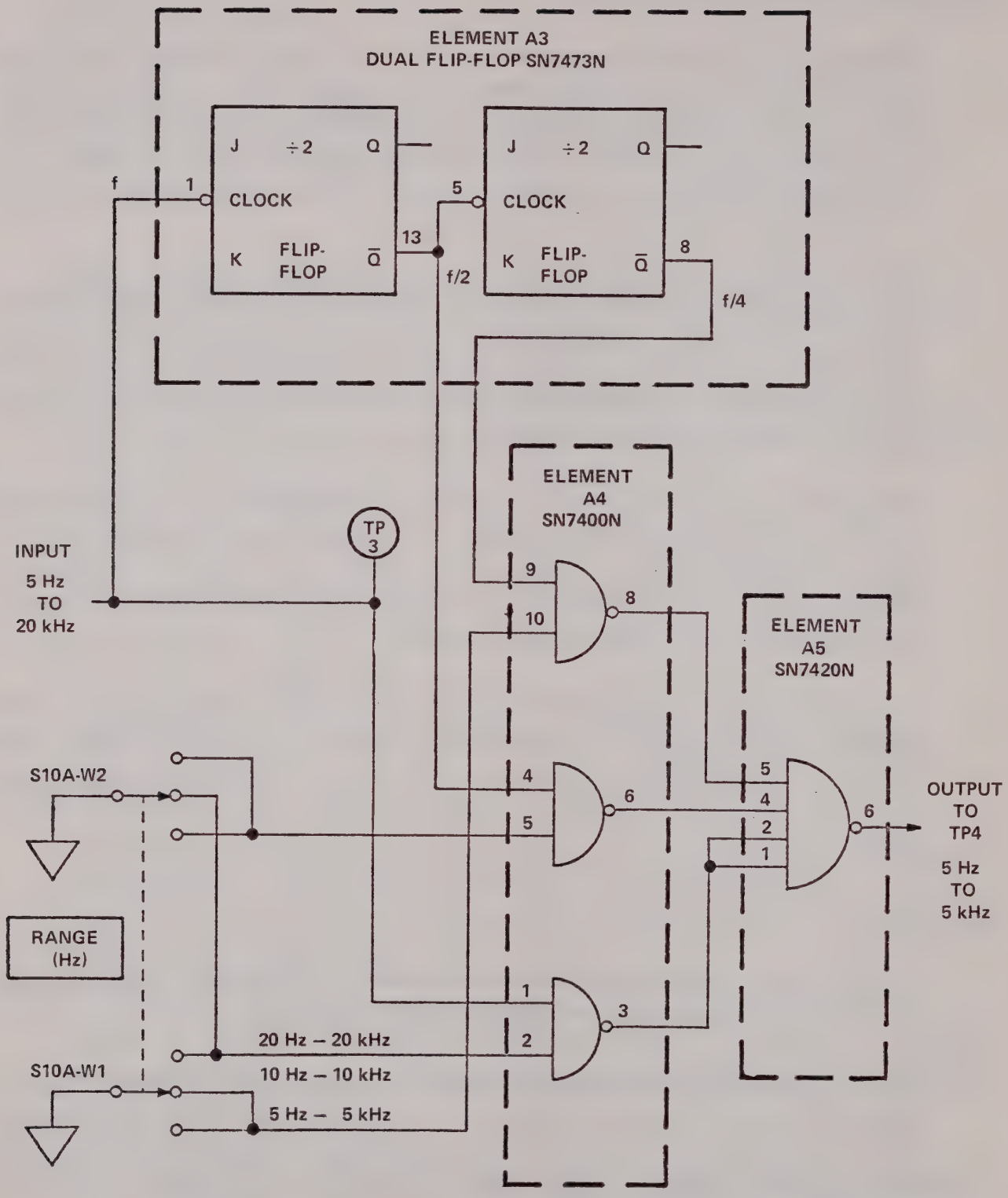


Figure 3-4. Logic Diagram of Range Switching (Frequency Division) Circuitry

With X-CAL switch S9A set to UPPER, an internal 2-kHz multivibrator is activated and its output is applied directly to the one-shot input (TP4, base of Q10). Because the upper frequency limit of the circuitry from this point to the output (TP18) is 5 kHz (refer to paragraph 3.3.3), the dc $\propto$ log frequency will be 0.867V at TP18 for any setting of RANGE (Hz) switch S10A.

The 2-kHz multivibrator comprises Q6, Q7, CR3, C12, C13 and R23 through R28. With S9A set to UPPER, +5V from emitter of Q8 (voltage regulator) is routed through A5-J to S9A-W2 (UPPER), through A5-K, R27 and R26 to the base of Q7. In this condition, the multivibrator oscillates at 2 kHz. The 2-kHz output at TP16 is routed through A5-6, S9A-W3 (UPPER), and A5-7 to the one-shot input at TP4.

3.3.5 One-Shot and ÷2 Flip-Flop

See Figure 3-2 and note that the one-shot and ÷2 flip-flop generate the basic pulses used to develop the two ramps, and then transfer their peak amplitude (dc $\propto$ 1/f) into the hold capacitor for subsequent log conversion.

Q10 and Q11 operate as a collector-coupled one-shot multivibrator; Q12 determines the pulse output voltage swing from 0V to +5V. See Figure 3-1 and note that each positive-going zero-crossing input (TP4) produces a 6-μs pulse (TP5). The 6-μs pulses drive ÷2 flip-flop element A6. The outputs of element A6 (Q and $\overline{Q}$) change state only on the negative-going input; i.e., at one-half the TP4 input frequency. Therefore Q and $\overline{Q}$ are alternately in a positive (+4V) state for the time equal to the period (1/f) of the input frequency at TP4. This technique is the basis for developing the two ramps, alternately, with their peak amplitude dc $\propto$ 1/f.

The output of the one-shot (TP5) is NAND'ed with $\overline{Q}$ (element A6-6) in element A7 (pins 10 and 9). The NAND'ed output at A7-8 is inverted by NAND element A7-13, -12 and -11. This overall connection performs the AND function; i.e., the output at A7-11 (TP7) is a logic "1" only when TP5 and $\overline{Q}$ are positive (logic "1" level). This train of $\approx$6-μs pulses at TP7 is subsequently scaled to produce TP8 which controls the sampling of ramp No. I peak amplitude (described in paragraph 3.3.6.1).

The output of the one-shot (TP5) is also NAND'ed with Q (element A6-8) in element A7 (pins 1 and 2), and inverted by element A7-4, -5 and -6. This logic produces the waveform at TP13. This train of $\approx$6-μs pulses at TP13 is subsequently scaled to produce the input to Q18-gate which controls the sampling of ramp No. II peak amplitude (described in paragraph 3.3.6.2).

3.3.6 Ramp Generators

3.3.6.1 Ramp No. I

Q19 inverts and scales the +4V to +0.4V waveform at TP6 to the 0V to −15V waveform at TP9 (collector of Q19 and gate of Q20). With 0V input to Q20 gate, Q20 source-to-drain resistance is about 30 ohms, which shunts (discharges) ramp storage capacitor C20. When Q20 gate (TP9) goes to −15V, the source-to-drain resistance is almost infinite, and C20 charges linearly as supplied by Q21, a constant current source. Thus, a linear ramp (TP10) is developed during the period of one cycle of the input frequency (at TP4).

When TP9 goes to 0V, C20 is again shunted and discharged. Note, however, that just prior to this point, the ramp amplitude is proportional to the period of the TP4 input frequency, or, is proportional to the reciprocal of frequency (1/f).

3.3.6.2 Ramp No. II

Q13 inverts and scales the +4V to +0.4V waveform at TP12 to 0V to −15V at TP14 (collector of Q13 and gate of Q15). When input to Q15 gate is 0V, the source-to-drain resistance is approximately 30 ohms, which shunts (discharges) ramp storage capacitor C18. When input to Q15 gate goes to −15V, the source-to-drain resistance is almost infinite, thus C18 charges linearly as supplied by Q14, a constant current source. Thus, a linear ramp (TP15) is developed during the period of one cycle of the input frequency (at TP4).

When TP14 goes to 0V, C18 is shunted and discharged. Note, however, that just prior to this point, the ramp amplitude is proportional to the TP4 input frequency period, or is proportional to the reciprocal of frequency (1/f).

3.3.7 Sample, Transfer and Hold

3.3.7.1 Ramp No. I

Observe waveform TP7 and note that its positive-going leading edge occurs about 6 μs before the end of the ramp peak. This 4V to 0.4V waveform (TP7) is scaled by Q23 and Q22 to the −15V to 0V waveform at TP8. which is applied to the gate of Q24. Therefore, Q24 is turned on and transfers the last 6 μs of peak ramp voltage from C20 into C24, the "hold capacitor". Note that waveforms TP9 and TP10 are both delayed approximately 1 μs; this is caused by C19 (base to emitter of Q19). This 1-μs delay allows the sampling pulse (TP8) to turn off Q24 about 1 μs before Q20 turns on and discharges C20.

3.3.7.2 Ramp No. II

During the last 6 μs of each alternate TP4 input cycle, Q18 is turned on and transfers the peak ramp voltage from C18 into "hold capacitor" C24. Waveform TP13 is developed by AND'ing TP5 (one-shot output) and TP12 (Q output from A6-8) in series NAND gates A7 (terminals 1 through 6). Waveform TP13 (4V to 0.4V) is scaled by Q17 and Q16 to the -15V to 0V waveform applied to Q18-gate. Note that waveforms TP14 and TP15 are both delayed approximately 1 μs; this is caused by C17 (base to emitter of Q13). This 1-μs delay allows the sampling pulse at TP13 to turn off Q18 about 1 μs before Q15 turns on and discharges C18.

3.3.8 D-C Buffer Amplifier

The voltage (dc $\propto$ 1/f) stored in "hold capacitor" C24 is buffered by an operational follower amplifier for application to the log converter circuit. This amplifier comprises differential pairs Q25 and Q27, and emitter follower Q28. Q26 provides a constant current source for Q25. Having greater than 10^9 ohms input impedance, the input gate of Q25 offers almost no load to C24.

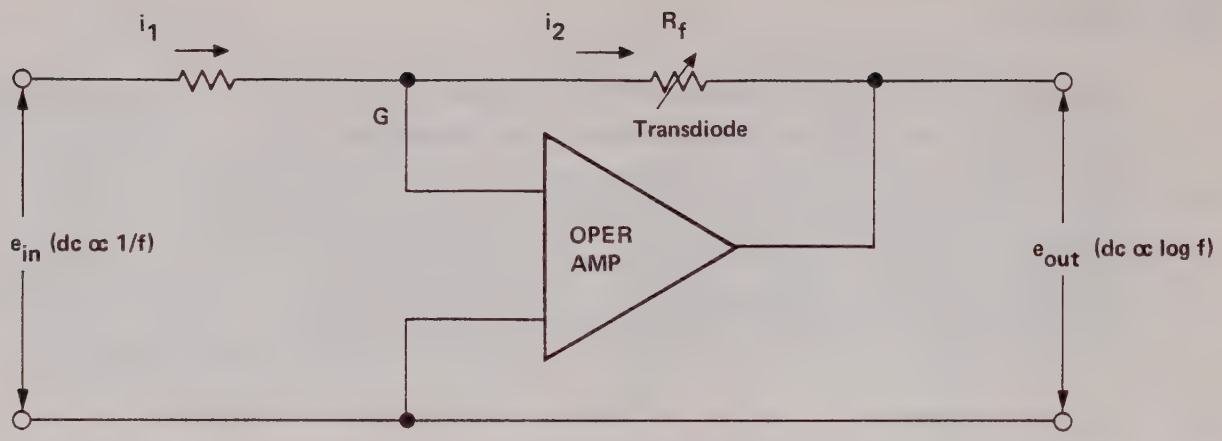
The 24V supply for Q25 and Q27 is developed from the 38V unregulated input at pin M. The 38V is filtered by R72, C25 and R73, and then regulated to +24V by 9V zener diode CR12 which is referenced to the +15V regulated supply.

The small high-frequency "spikes" shown on TP11 waveform (output of Q28) are switching transients caused by Q18 and Q24; they are non-affective. The output of Q28 (dc $\propto$ 1/f) is fed to the log converter circuit.

3.3.9 Log Converter

The log converter circuit consists of an operational amplifier (differential pairs Q29 and Q31, and emitter follower Q32), a transdiode (diode-connected transistor, element A8 terminals 2, 3 and 4), and associated circuitry. Q30 provides a constant current source for Q29.

Q29, Q31 and Q32 operate as a conventional operational amplifier except that the overall gain is controlled by the feedback through transdiode element A8. Because the impedance of a transdiode varies inversely and logarithmically as the current forced through it, the overall gain of the operational amplifier is caused to vary inversely and logarithmically. Therefore, because the gain of an operational amplifier is equal to the feedback impedance divided by the input impedance (gain = $\frac{R_{FB}}{R_{IN}}$), and the transdiode impedance is varying inversely and logarithmically to the input, the voltage developed at the output is proportional to the log of the input. This function is illustrated as follows:



Q29, Q31 and Q32 operate as a conventional operational amplifier with a transdiode substituted for a R_f. Therefore, to maintain ground potential at the summing junction (point G), the input current (i_1) must equal the output current (i_2). Because R_f is a transdiode (whose impedance varies logarithmically as the current passed through it), i_2 (= i_1) is proportional to the antilog of e_{out}. Also, because $i_2 = i_1 = e_{in}/R_{in}$, e_{in} is proportional to the antilog of e_{out}; or e_{out} is proportional to the log of e_{in}. This logic is given in brief mathematical form as follows:

$$i_2 \propto \exp e_{out}$$

or $\quad e_{out} \propto \log i_2$ (from basic diode equation, neglecting temperature changes)

but $\quad i_2 = i_1 = e_{in}/R_{in}$

therefore $\quad e_{out} \propto \log e_{in}/R_{in} \propto \log e_{in}$

or $\quad e_{out} \propto \log e_{in}$

The transdiode element is contained in an oven, along with a second diode-connected transistor that has identical operating characteristics. The DC ∝ log f (output of Q32 at junction of R91, C29 and A8-10) passes through this second diode which provides an offset to cancel the "constant of proportionality" (K) of the log converter. The voltage at TP17 is therefore equal to log f. This voltage is applied to the output buffer amplifier.

Note that because the log converter diode and offset diode are on the same "chip" in the same oven, both are equally affected by any temperature change and thus compensate each other equally.

3.3.10 Output Buffer Amplifier

The output buffer amplifier consists of element A9, emitter follower Q33, and associated circuitry, connected as an operational amplifier. CR14 and CR15 provide input overload protection. The overall gain is approximately 40. Q33 provides ample current at both the 1 VOLT and 0.1 VOLT output connectors to drive external recording equipment. The outputs are short-circuit proof with a nominal output impedance of 500 ohms (1 VOLT output) and 50 ohms (0.1 VOLT output).

3.3.11 Power Supply Requirements

The log frequency converter card A5 receives all operating voltages (+15V, -15V and ≈+38V) from the SD112-H power supply circuit card A7. (See schematic DWG. NO. 10928 in the SD112-H Instruction Manual.)

SECTION IV

CALIBRATION AND MAINTENANCE

4.1 INTRODUCTION

This section contains calibration procedures and maintenance instructions for the log frequency converter circuit in the Model SD112-1-H Voltmeter/Frequency Log Converter. The instrument has been calibrated at the factory prior to shipment and should remain calibrated indefinitely. However, because of possible amplifier gain changes over long periods of operation, and when parts are replaced, the calibration should be checked periodically and adjustments made as necessary in accordance with the procedure of Paragraph 4.2. If proper operation cannot be achieved, refer to Paragraph 4.3 for troubleshooting techniques. See also the Model SD112-H Instruction Manual, Section IV, for general maintenance information. The test equipment required for maintenance of the log frequency converter circuits is listed in Table 4-1.

Before calibrating or troubleshooting, the technician is advised to study carefully the theory of operation in Section III, and Figures 1-2 and 1-3 in Section I which describe the front and rear panel controls, indicators and connectors. See also the schematic and circuit card component layout drawing located in the back of this addendum. For parts replacement information, refer to paragraph 4.4.

A complete and detailed calibration procedure, based on the factory final checkout procedure, is given in paragraph 4.5.

Table 4-1. Test Equipment Required

Name	Model No.	Manufacturer
Digital Voltmeter	3440A	Hewlett-Packard
Frequency Counter	5223L	Hewlett-Packard
Oscilloscope	561A	Tektronix
Time Base Plug-In	Type 67	Tektronix
Wideband Calibrated Preamp Plug-In	Type 3A6	Tektronix
10 Megohm Probe	P6008	Tektronix
Pulse Generator	101	Datapulse
Sweep Oscillator	SD104A	Spectral Dynamics

4.2 PERIODIC CALIBRATION PROCEDURE

4.2.1 Preliminary Setup

If only the log frequency converter circuit card A5 is to be calibrated (i.e., not as a part of the overall SD112-1-H calibration), perform the following preliminary procedures:

a. Set the SD112-1-H on a test bench, remove the six screws holding the chassis top cover plate, and remove the cover.

b. Set RANGE (Hz) switch to 5-5K, and X-CAL switch to OPER. (Except for the power switch, all other SD112-1-H controls do not affect the log frequency converter operation.)

c. Using circuit card extender assembly (23060-1), extend circuit card A5 with parts oriented in proper direction and then apply power.

NOTE

Allow instrument to warm up for at least 5 minutes.

d. Connect DVM to A5CR12 cathode (bottom lead), and measure +25V ±2V.

4.2.2 Periodic Calibration

NOTE

Throughout the following procedures, the frequency period is given in parenthesis after each calibration frequency.

a. 2-kHz Oscillator

1) Set X-CAL switch to UPPER.

2) Connect frequency counter to A5TP16.

3) Measure 2 kHz ±1 Hz (500 μs ±0.25 μs). Adjust A5R27 as necessary for proper frequency.

4) Set X-CAL switch to OPER.

b. Sample and Hold Circuit

Remove power, remove A5Q18, and reapply power. Connect SD104A and frequency counter to LOG FREQ INPUT J2. Adjust SD104A for 1 Vrms sine wave output, at frequency of 50 Hz ±0.005 Hz (20 ms ±0.02 ms). Connect DVM to A5TP11.

1) Adjust A5R58 as necessary for DVM reading of 1V ±10 mV at A5TP11.

2) Change INPUT frequency to 5 kHz ±5 Hz (200 μs ±0.2 μs), and adjust A5R65 for 10 mV ±0.1 mV at A5TP11.

3) Because some interaction exists, repeat steps 1) and 2) as necessary to obtain proper readings.

4) Change input frequency to 5 Hz ±0.005 Hz (200 ms ±0.2 ms); measure 10V ±0.1V. If voltage is incorrect, repeat steps 1), 2) and 4) for "best fit" in-spec readings.

5) Remove power, re-insert A5Q18, and reapply power.

c. Log Converter

1) Adjust SD104A for frequency of 5 Hz ±0.005 Hz (200 ms ±0.2 ms). Connect DVM to A5TP18.

2) Note equal incremental voltage changes between input frequencies of 5 Hz and 50 Hz, 50 Hz and 500 Hz, and 500 Hz and 5 kHz. If necessary, adjust A5R81 for equal incremental voltage changes (±2%).

d. Output Voltage

1) Adjust SD104A for frequency of 5 kHz ±5 Hz (200 μs ±0.2 μs).

2) Measure 10V ±24 mV at A5TP18. Adjust A5R105 as necessary for proper reading.

3) Adjust SD104A to 5 Hz ±0.005 Hz (200 ms ±0.2 ms).

4) Measure 0V ±24 mV at A5TP18. Adjust A5R94 as necessary for proper reading.

5) Interaction exists between the adjustments of steps 2) and 4); repeat steps 1) through 4) as necessary to obtain proper readings.

e. Output Linearity Check

Check for the proper d-c voltage at A5TP18 for each of the following frequencies:

INPUT FREQ (Hz)		PERIOD		VOLTAGE AT A5TP18		
5,000	±5	200 μs	±0.2 μs	9.976V	to	10.024V
1,581	±1.6	632.5 μs	±0.633 μs	8.309V	to	8.357V
500	±0.5	2 ms	±0.002 ms	6.642V	to	6.690V
158.1	±0.16	6.325 ms	±0.0063 ms	4.976V	to	5.024V
50	±0.05	20 ms	±0.02 ms	3.309V	to	3.357V
15.81	±0.016	63.25 ms	±0.0633 ms	1.642V	to	1.690V
5.00	±0.005	200 ms	±0.2 ms	−24 mV	to	+24 mV

f. X-CAL Check

1) Set X-CAL switch to UPPER, and measure 8.667V ± 50 mV at A5TP18.

2) Set X-CAL to LINE. Sequentially set RANGE (Hz) switch to 5-5K, 10-10K and 20-20K; and measure 3.6V, 2.6V and 1.6V (all ± 24 mV) respectively at A5TP18.

4.3 TROUBLESHOOTING

A part failure will normally be indicated by incorrect or the absence of LOG FREQ OUTPUT voltage. The X-CAL switch provides a quick operational check. (See the functional block diagram of Figure 3-2, the associated test point waveforms in Figure 3-1, and the schematic diagram in the back of this addendum.) The following steps should help localize a fault to a particular circuit.

a. Perform the Preliminary Setup procedure of paragraph 4.2.1; ensure that all d-c operating voltages are correct.

b. Set X-CAL switch to LINE and connect DVM to A5TP18. Sequentially set RANGE (Hz) switch to 5-5K, 10-10K and 20-20K; and measure 3.6V, 2.6V and 1.6V (all ±24 mV) respectively at A5TP18.

If these voltages are correct, suspect trouble in the external cabling and ancillary equipment in the system. If none of the voltages are correct, perform step c., otherwise proceed to step d.

c. Set X-CAL switch to UPPER and measure 8.667V ±50 mV at A5TP18.

If this voltage is correct, the circuits between A5TP4 and A5TP18 are operating properly; in this case, suspect trouble between A5TP1 and A5TP4 and perform step d.

d. Set X-CAL to LINE. Using standard troubleshooting techniques, check for proper waveforms and voltages between A5TP1 and A5TP4 for each setting of the RANGE (Hz) switch.

If the 5-5K RANGE (Hz) setting is correct, but the 10-10K 20-20K do not operate, check the applicable NAND gate and frequency dividing flip-flop(s).

If the UPPER X-CAL output voltage is absent or incorrect, first suspect the 2-kHz oscillator. Perform step e.

e. With X-CAL set to UPPER, connect frequency counter to A5TP16 and measure 2-kHz ±1 Hz. This frequency should also be at A5TP4.

If the waveform at A5TP4 is correct, continue checking for proper waveforms at all test points (see Figures 3-1 and 3-2), and for proper voltages (see the schematic diagram) between A5TP4 and A5TP18.

It is sometimes desirable to check the operation of each ramp circuit separately. To disable ramp No. II while checking No. I, remove power, remove A5Q18, and then reapply power. In like manner, ramp No. II can be checked by removing A5Q24. In either case, be sure to return the transistor to its socket after completion of circuit troubleshooting.

After the trouble has been eliminated, perform the periodic calibration procedure of paragraph 4.2. If the voltages at A5TP18 are out of specification (paragraph 4.2, steps e. and f.), perform the detailed calibration procedure of paragraph 4.5 in its entirety.

4.4 PARTS REPLACEMENT

Except for some special SDC Specification-controlled parts listed in Table 4-2, which must be ordered from Spectral Dynamics Corporation, standard electronic parts have been used throughout the instrument. Spectral Dynamics Corporation maintains a complete stock of all parts and the complete printed circuit card, Log Frequency Converter Assembly 11160-1.

Table 4-2. Special Replaceable Parts List

Reference Designator	Description	Part Number Mfr. Designation
A5	Log Freq Converter Circuit Card Assembly	11160-1
Q1,Q2	2N3391A (Factory selected pair)	20013-044A
	Knob, RANGE (Hz)	20013-176
	Knob, X-CAL	20013-177

When ordering a replacement part or assembly, be sure to include the reference designation, the part number or manufacturers designation, and a complete description; include also the instrument name, model number, and serial number.

4.5 DETAILED CALIBRATION PROCEDURE

This calibration procedure is the procedure used by the factory during final checkout and calibration of the Log Frequency Converter Assembly 11160-1. The test equipment required is listed in Table 4-1; test equipment having equal or better characteristics may be substituted. See the schematic diagram and component layout drawing in the back of this addendum for the location of all calibration controls and test points; note that the test points are identified on the parts side of the circuit card.

a. Preliminary Setup – Perform the preliminary setup procedure of paragraph 4.2.1 in its entirety.

b. 2-kHz Oscillator

1) Set X-CAL to UPPER; connect frequency counter to A5TP16.

2) Adjust A5R27 for 2 kHz ±1 Hz (500 μs ±0.25 μs).

3) Set X-CAL to OPER.

c. Sample and Hold Circuits

Remove power, remove A5Q18, and reapply power. Connect SD104A and frequency counter to LOG FREQ INPUT J2. Adjust SD104A for 1 Vrms sine wave output, at frequency of 50 Hz ±0.005 Hz (20 ms ±0.02 ms). Connect DVM to A5TP11.

1) Adjust A5R58 for DVM reading of 1V ±10 mV.

2) Change INPUT frequency to 5 kHz ±5 Hz (200 μs ±0.2 μs), and adjust A5R65 for 10 mV ±0.1 mV.

3) Because some interaction exists, repeat steps 1) and 2) as necessary to obtain proper readings.

4) Change input frequency to 5 Hz ±0.005 Hz (200 ms ±0.2 ms); measure 10V ±0.1V. If voltage is incorrect, repeat steps 1), 2) and 4) for "best fit" in-spec readings.

5) Reinsert A5Q18.

d. Ramp Adjust

1) Change frequency to 50 Hz ±0.05 Hz (20 ms ±0.02 ms), and connect oscilloscope to A5TP11.

2) Adjust A5R46 for minimum ripple. (This equalizes the amplitudes of ramps I and II.)

3) Again check steps 1), 2) and 4) of procedure c. for in-spec readings.

4) Measure <100 mV p-p ripple at A5TP18.

e. Log Converter

1) Adjust SD104A for frequency of 5 Hz ±0.005 Hz (200 ms ±0.2 ms).

2) Adjust A5R81, A5R94, and A5R105 to midrange (approximately 12-1/2 turns from either end).

3) Connect DVM to A5TP18.

4) Note incremental voltage changes as input frequency is changed between 5 Hz and 50 Hz, 50 Hz and 500 Hz, and 500 Hz and 5 kHz. Adjust A5R81 as necessary for equal (±2%) incremental voltage changes.

f. Output Voltage

1) Adjust SD104A for frequency of 5 kHz ±5 Hz (200 μs ±0.2 μs).

2) Adjust A5R105 for 10V ±24 mV at A5TP18.

3) Adjust SD104A to 5 Hz ±0.005 Hz (200 ms ±0.02 ms).

4) Adjust A5R94 for 0V ±24 mV at A5TP18.

5) Interaction exists between adjustments of steps 2) and 4); repeat steps 1) through 4) as necessary to obtain proper readings.

g. Output Linearity

1) Check the d-c voltage at A5TP18 for each of the following frequencies:

INPUT FREQ (Hz)		PERIOD		VOLTAGE AT A5TP18		
5,000	±5	200 μs	±0.2 μs	9.976V	to	10.024V
1,581	±1.6	632.5 μs	±0.633 μs	8.309V	to	8.357V
500	±0.5	2 ms	±0.002 ms	6.642V	to	6.690V
158.1	±0.16	6.325 ms	±0.0063 ms	4.976V	to	5.024V
50	±0.05	20 ms	±0.02 ms	3.309V	to	3.357V
15.81	±0.016	63.25 ms	±0.0633 ms	1.642V	to	1.690V
5.00	±0.005	200 ms	±0.2 ms	-24 mV	to	+24 mV

2) Set RANGE (Hz) switch to 10-10K and check the d-c voltage at A5TP18 for each of the following frequencies:

INPUT FREQ (Hz)		PERIOD		VOLTAGE AT A5TP18		
10,000	±10	100 μs	±0.1 μs	9.976V	to	10.024V
1,000	± 1	1 ms	±0.001 ms	6.642V	to	6.690V
100	± 0.1	10 ms	±0.01 ms	3.309V	to	3.357V
10	± 0.01	100 ms	±0.1 ms	-24 mV	to	+24 mV

3) Set RANGE (Hz) switch to 20-20K and check the d-c voltage at A5TP18 for each of the following frequencies:

INPUT FREQ (Hz)		PERIOD		VOLTAGE AT A5TP18		
20,000	±20	50 μs	±0.05 μs	9.976V	to	10.024V
2,000	± 2	500 μs	±0.5 μs	6.642V	to	6.690V
200	± 0.2	5 ms	±0.005 ms	3.309V	to	3.357V
20	± 0.02	50 ms	±0.05 ms	-24 mV	to	+28 mV

h. Response to Frequency Change

1) On SD112-1-H, set RANGE (Hz) switch to 5-5K. Connect SD104A to LOG FREQ INPUT (J2) of SD112-1-H.

2) On SD104A, set MULTIPLIER A to 1 and adjust for 50 Hz ±0.05 Hz.

3) Connect storage oscilloscope to A5TP18 and adjust horizontal sweep for 500 ms/cm.

4) On SD104A, switch MULTIPLIER A to 0.1 and note response time on oscilloscope; it should be 500 ms $\begin{pmatrix} +200 \text{ ms} \\ -300 \text{ ms} \end{pmatrix}$.

NOTE

Measure response time between 10 and 90% points.

i. X-CAL

1) Set X-CAL switch to UPPER, and measure 8.667V ±50 mV at A5TP18.

2) Set X-CAL to LINE. Sequentially set RANGE (Hz) switch to 5-5K, 10-10K and 20-20K; and measure 3.6V, 2.6V and 1.6V (all ±24 mV) respectively at A5TP18.

Step i. completes the detailed calibration procedure. Remove power; remove extender card and circuit card A5 from receptacle XA5. Replace circuit A5 and extender card in their respective proper locations. Replace instrument chassis top cover.

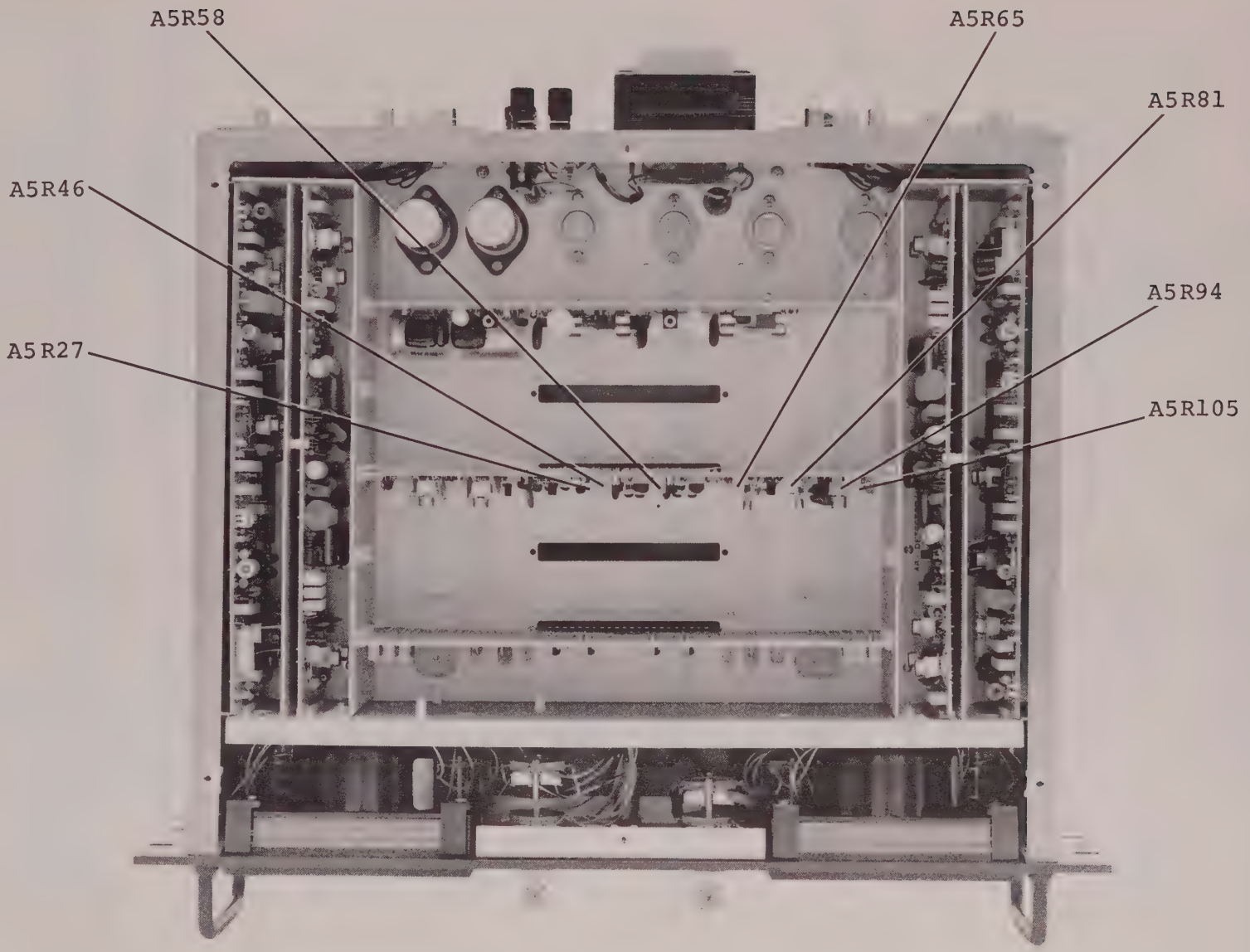


Figure 4-1. Top Chassis View — Calibration Controls (SD112-1-H Only)

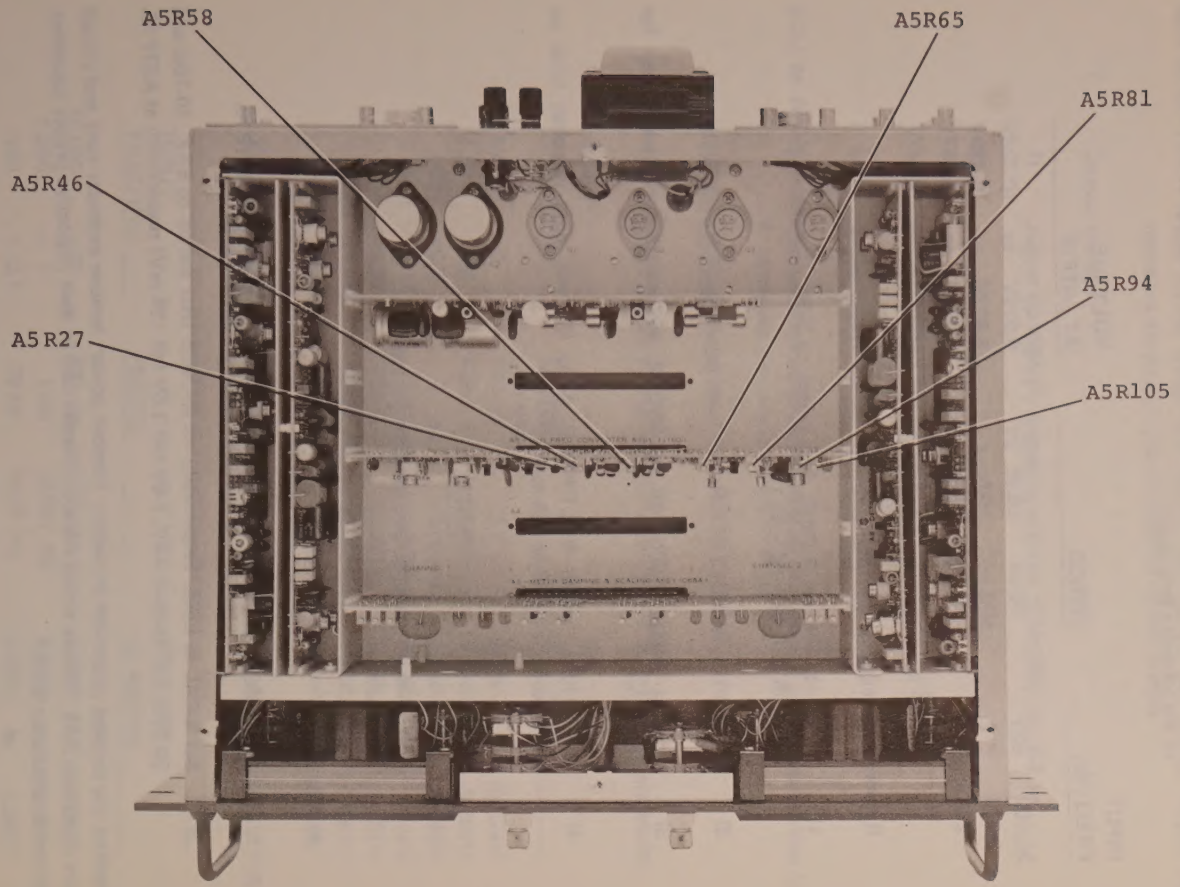


Figure 4-1. Top Chassis View — Calibration Controls (SD112-1-H Only)